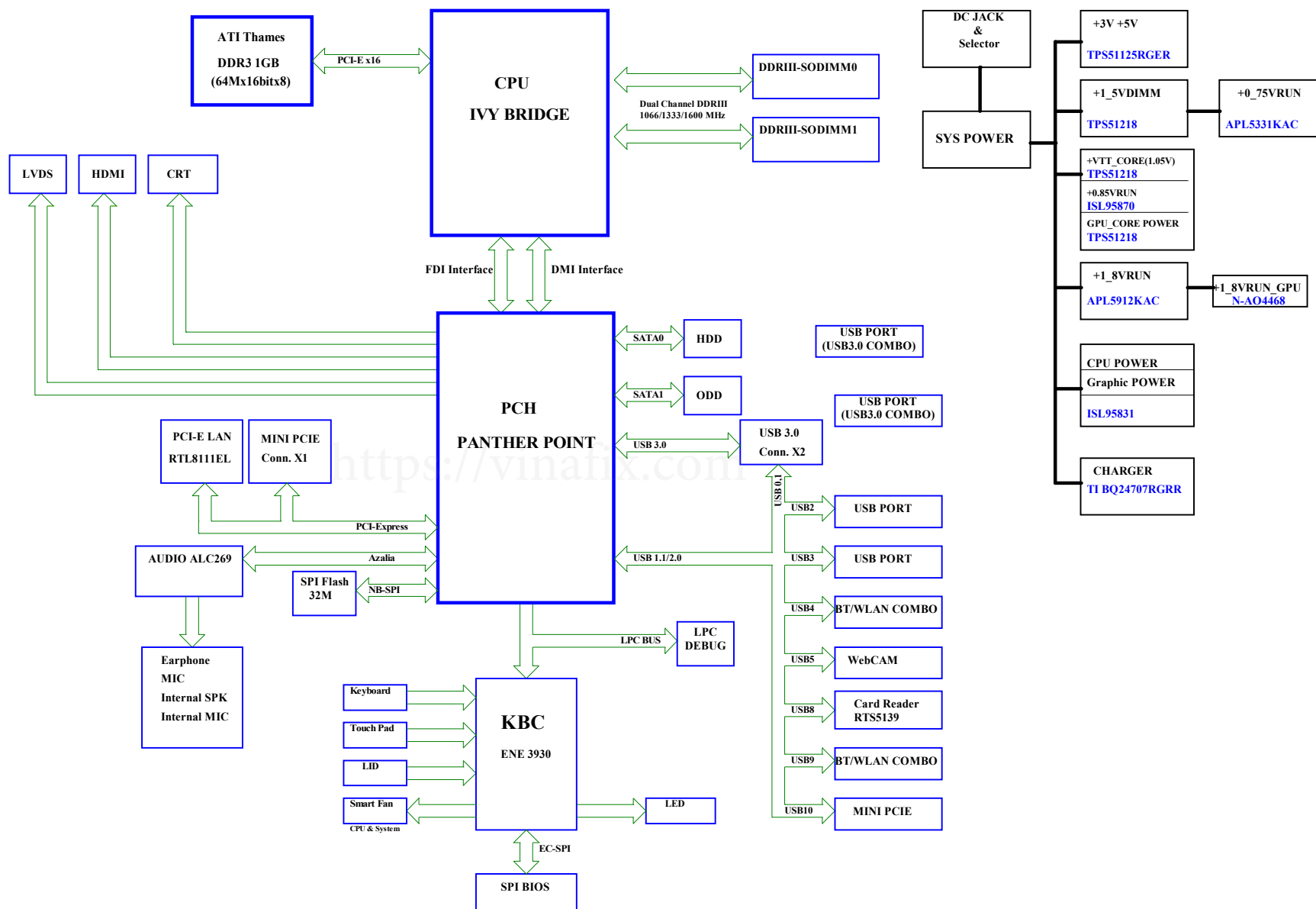
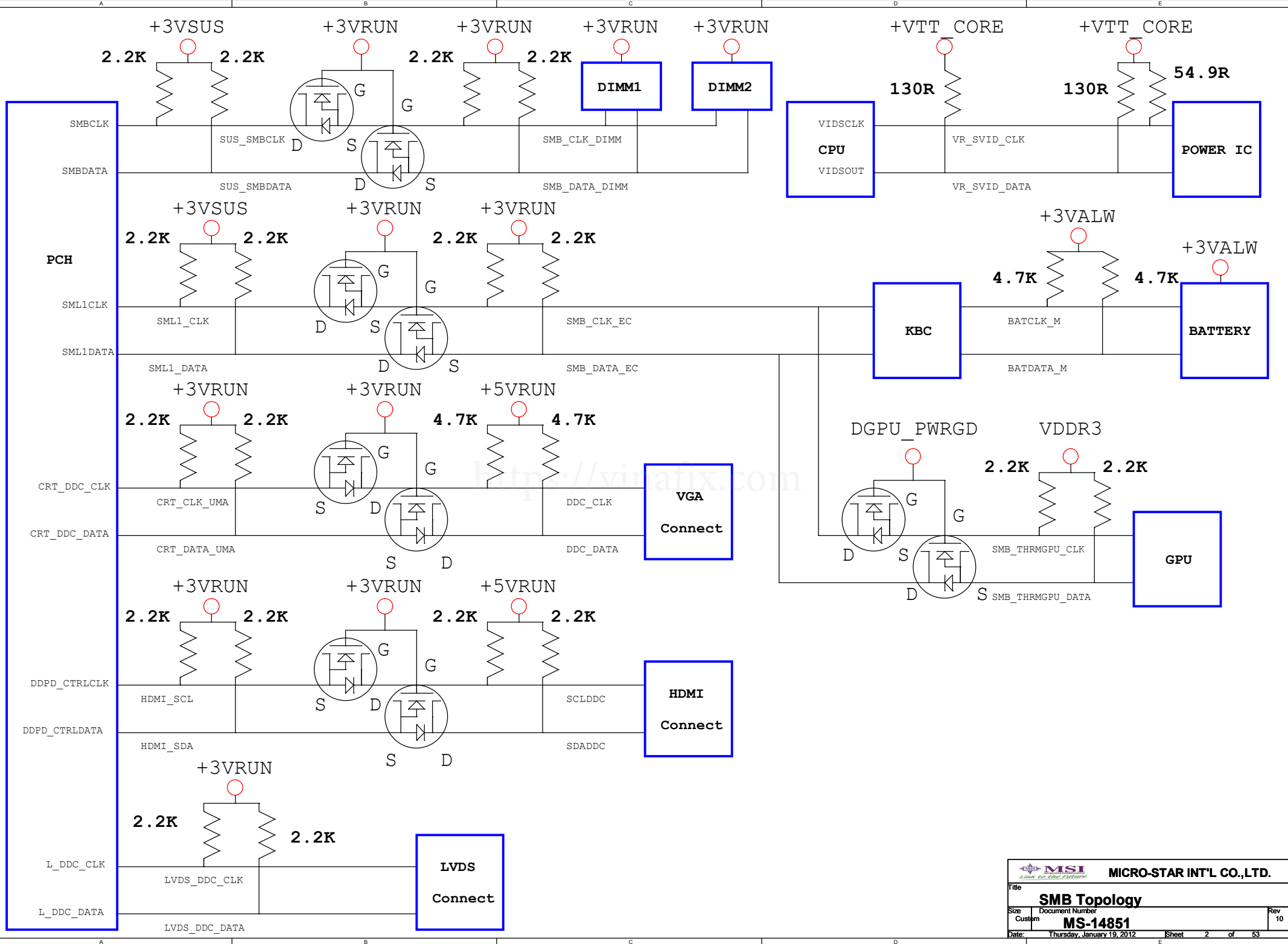


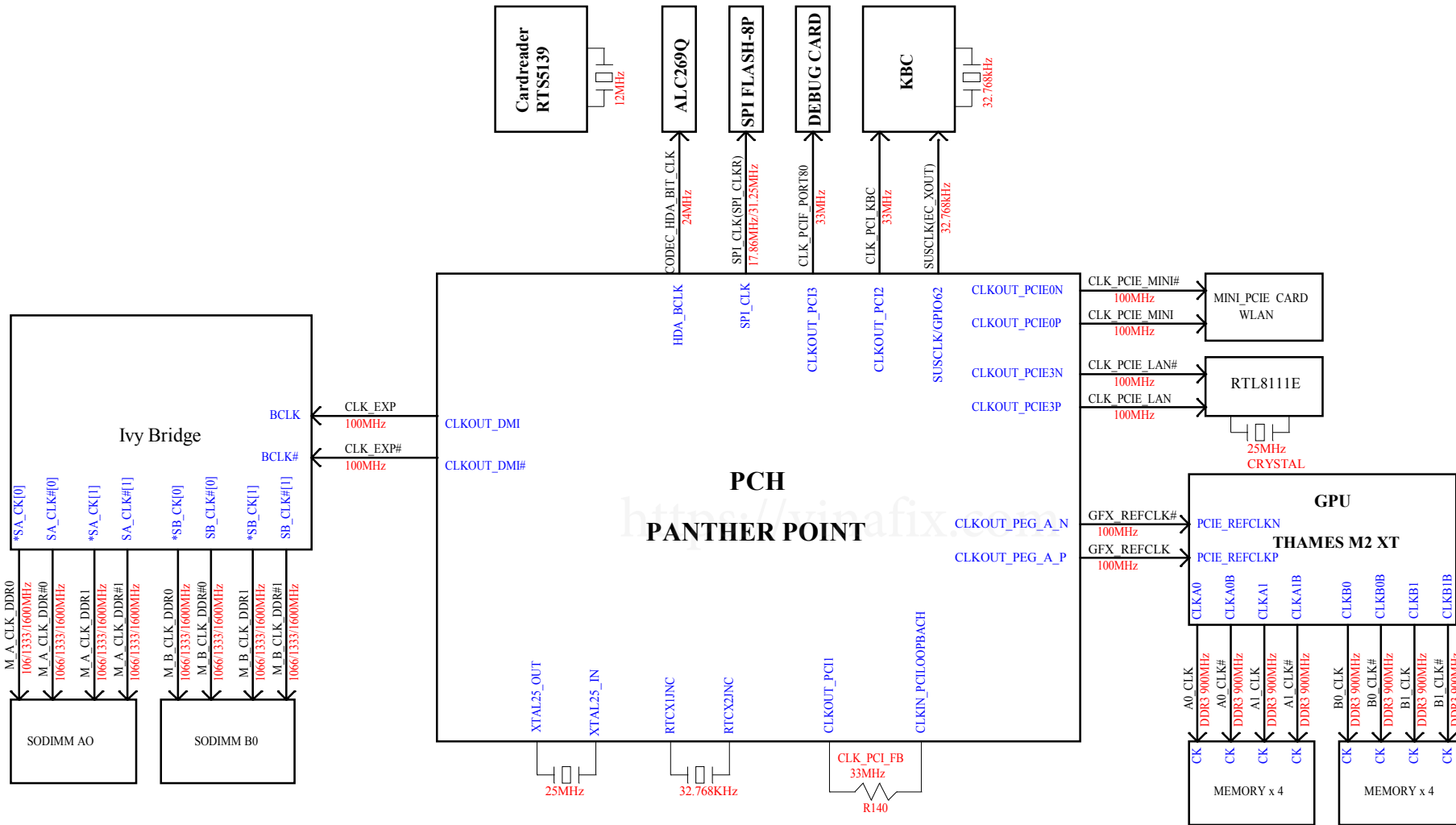
# Chief River Platform

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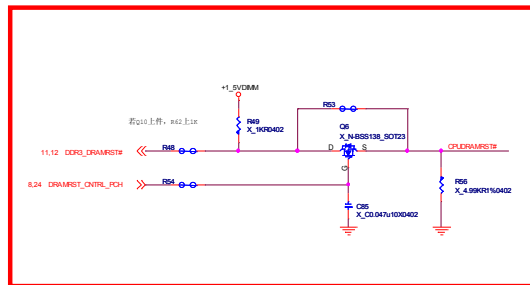
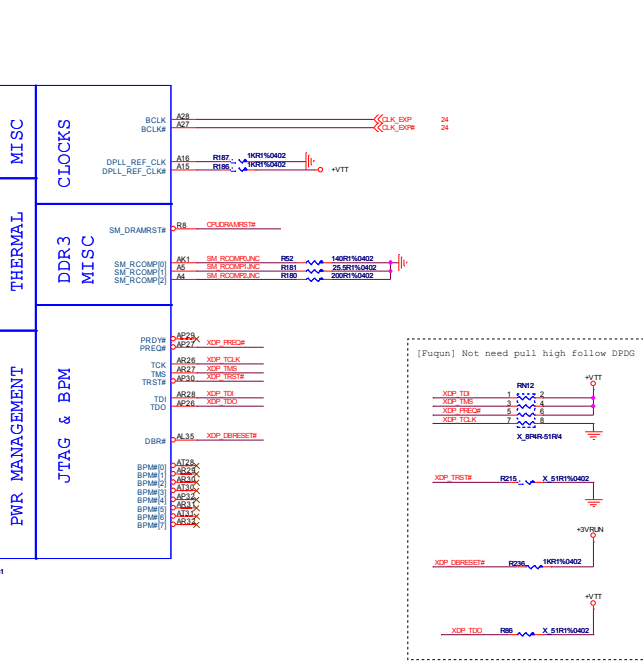








#### IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



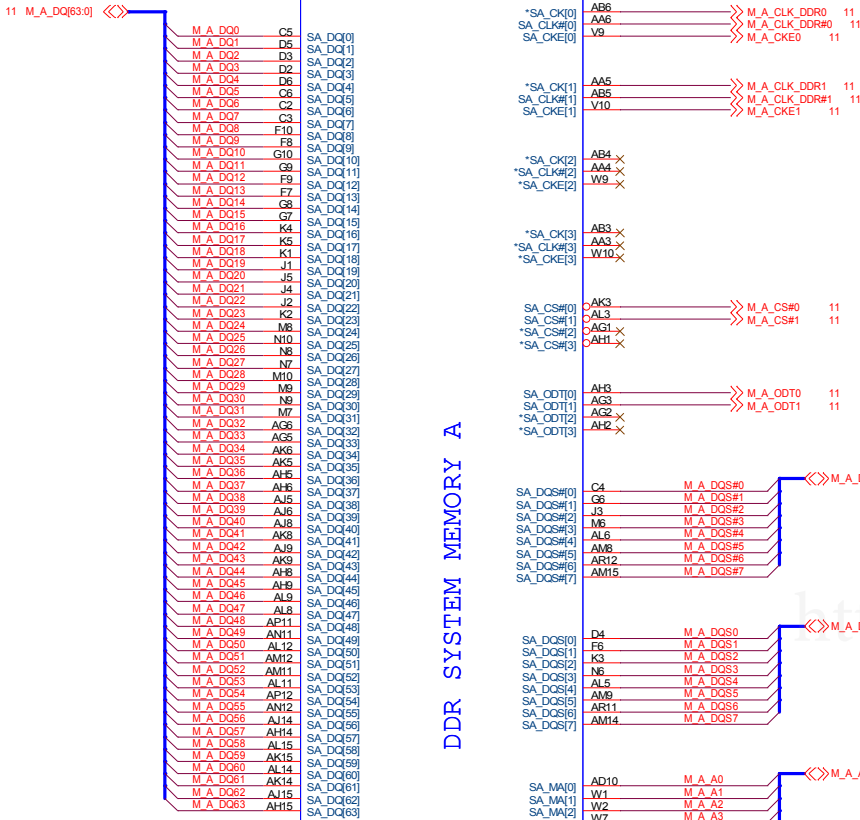
Vinafix.com

# IVY BRIDGE PROCESSOR (DDR3)

U21C

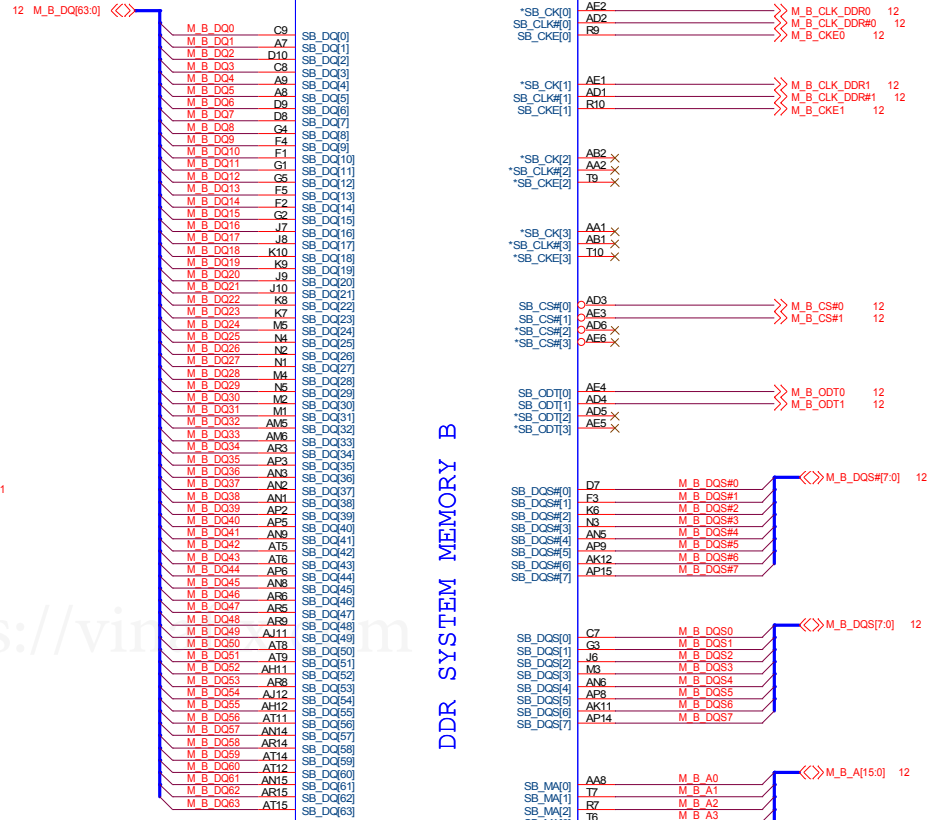
DDR SYSTEM MEMORY A

Ivy Bridge\_PGA\_2DPC\_Rev0p61



U21D

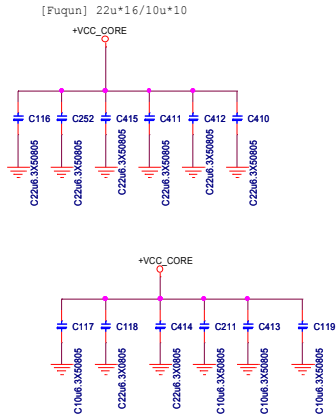
DDR SYSTEM MEMORY B



# IVY BRIDGE PROCESSOR (POWER)

[Fugun] 0.3~1.52V  
[Fugun] 45W----94A  
35W----52A

## POWER



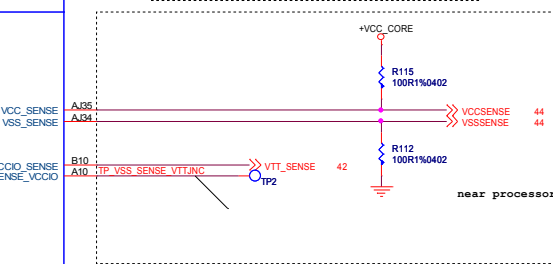
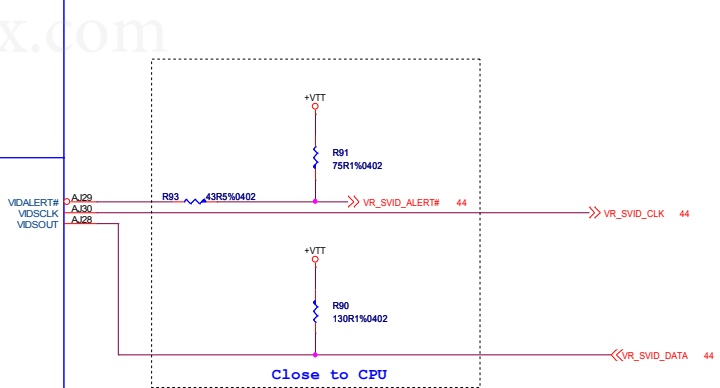
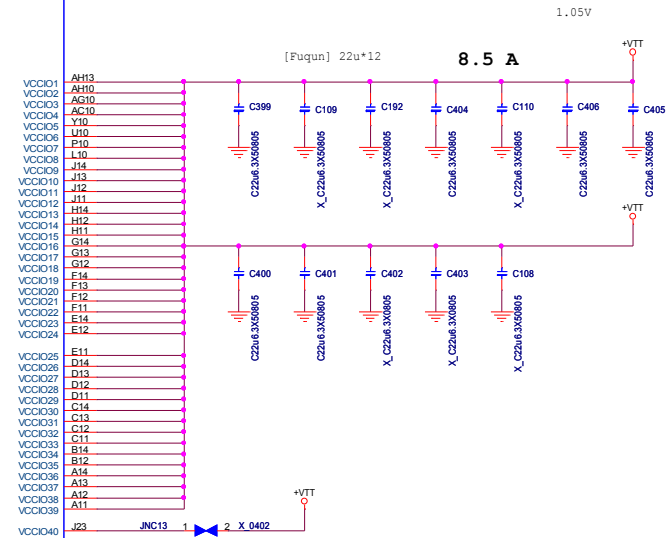
+VCC\_CORE  
52 A

U21F

AG35  
AG34  
AG33  
AG32  
AG31  
AG30  
AG29  
AG28  
AG27  
AG26  
AG25  
AG24  
AG23  
AG22  
AG21  
AG20  
AG19  
AG18  
AG17  
AG16  
AG15  
AG14  
AG13  
AG12  
AG11  
AG10  
AG9  
AG8  
AG7  
AG6  
AG5  
AG4  
AG3  
AG2  
AG1  
AG0  
VCC1  
VCC2  
VCC3  
VCC4  
VCC5  
VCC6  
VCC7  
VCC8  
VCC9  
VCC10  
VCC11  
VCC12  
VCC13  
VCC14  
VCC15  
VCC16  
VCC17  
VCC18  
VCC19  
VCC20  
VCC21  
VCC22  
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VCC73  
VCC74  
VCC75  
VCC76  
VCC77  
VCC78  
VCC79  
VCC80  
VCC81  
VCC82  
VCC83  
VCC84  
VCC85  
VCC86  
VCC87  
VCC88  
VCC89  
VCC90  
VCC91  
VCC92  
VCC93  
VCC94  
VCC95  
VCC96  
VCC97  
VCC98  
VCC99  
VCC100

## CORE SUPPLY

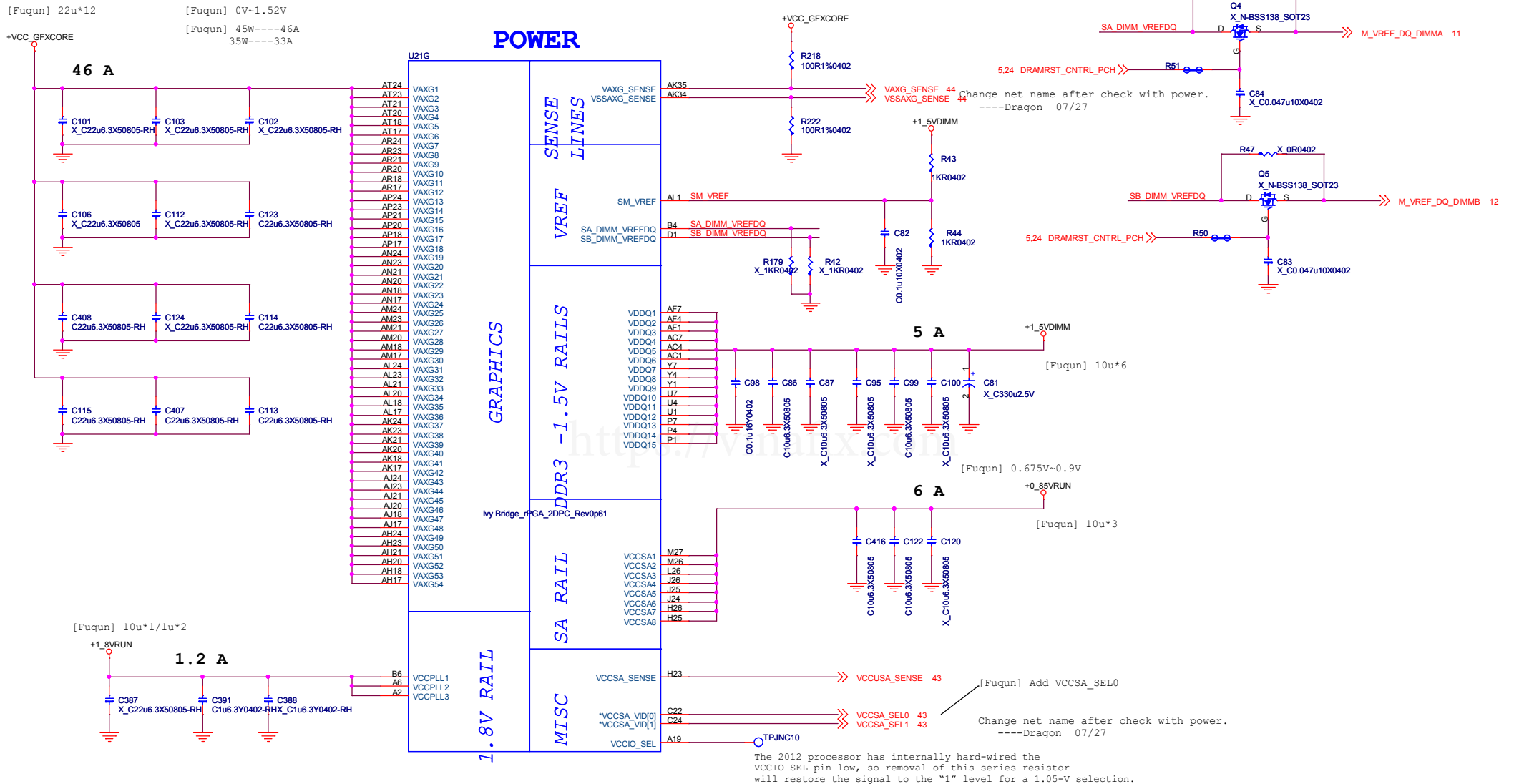
## PEG AND DDR



Ivy Bridge\_rPGA\_2DPC\_Rev0p61

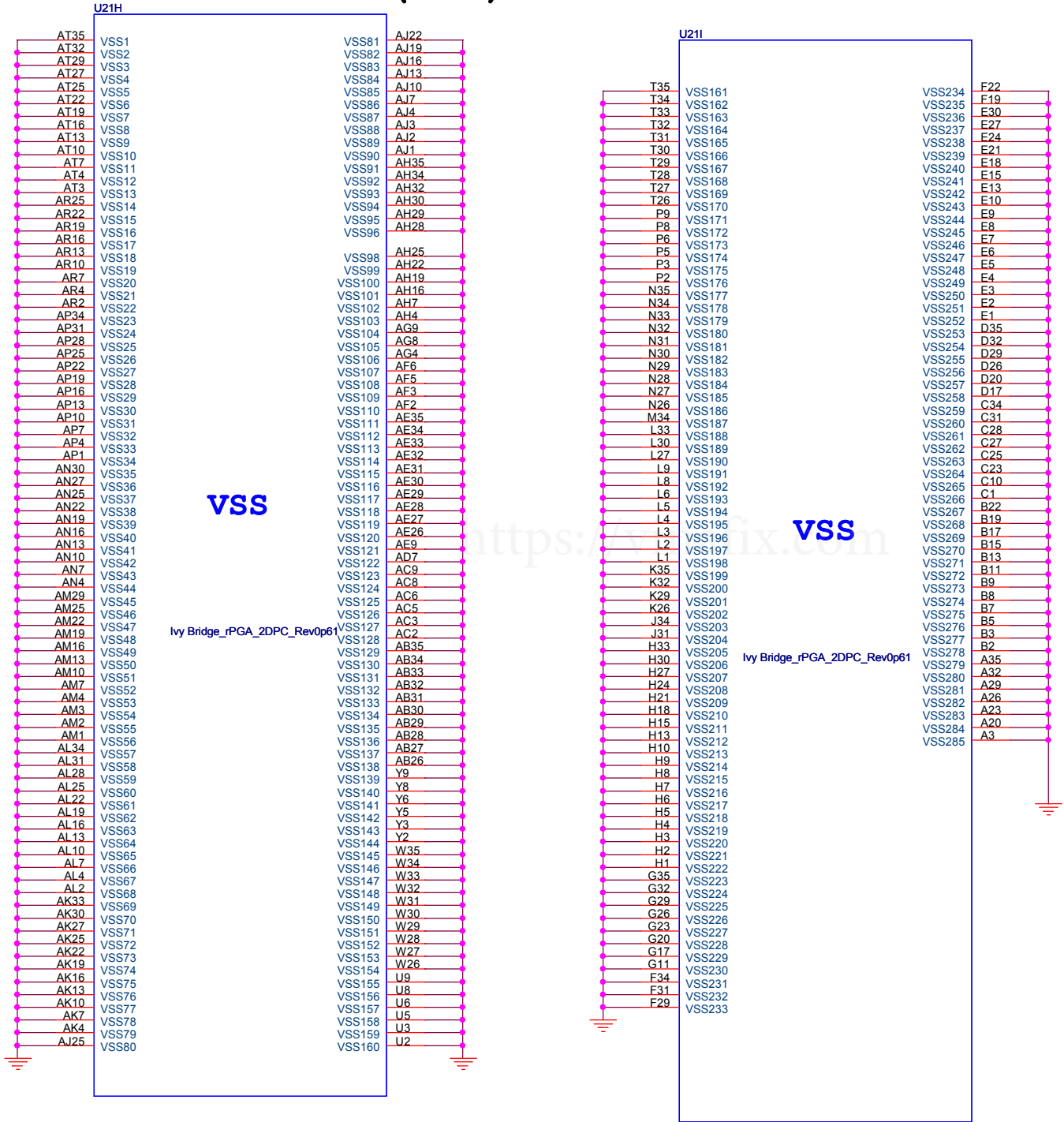
## IVY BRIDGE PROCESSOR (GRAPHICS POWER)

PPDG Recommend 100R






IVY BRIDGE PROCESSOR (GND)



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**MICRO-STAR INT'L CO.,LTD.**

Title

Ivy Bridge (GND)

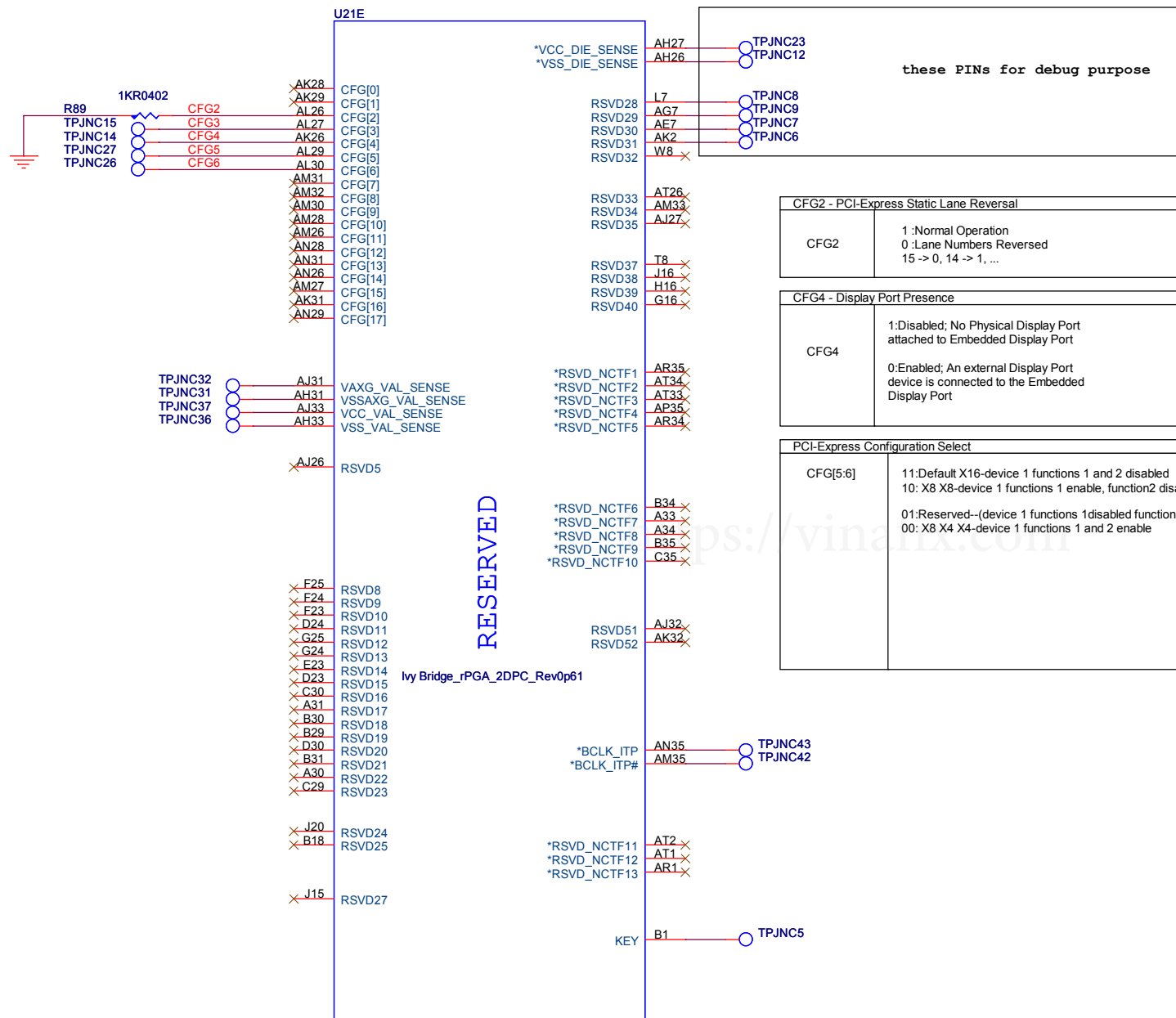
Size  
Custom

Document Number  
**MS-14851**

Rev  
10

Date: Thursday, January 19, 2012Sheet 9 of 53

# IVY BRIDGE PROCESSOR (RESERVED)

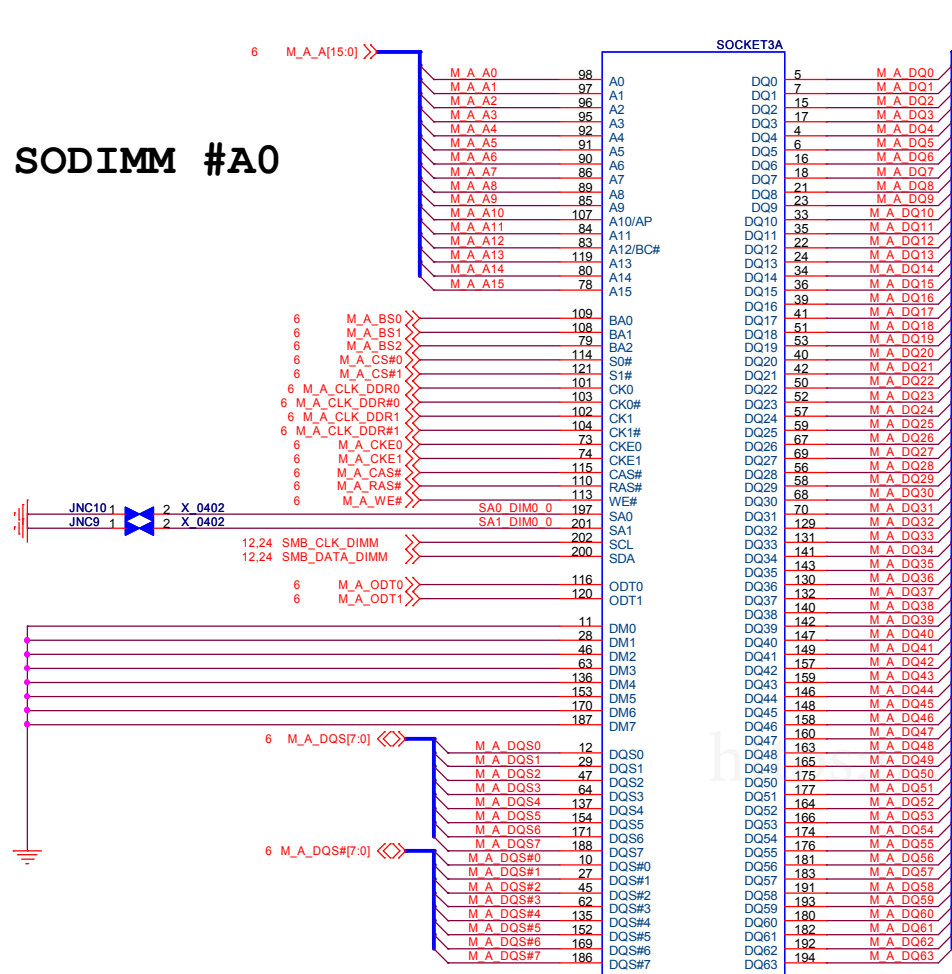


CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

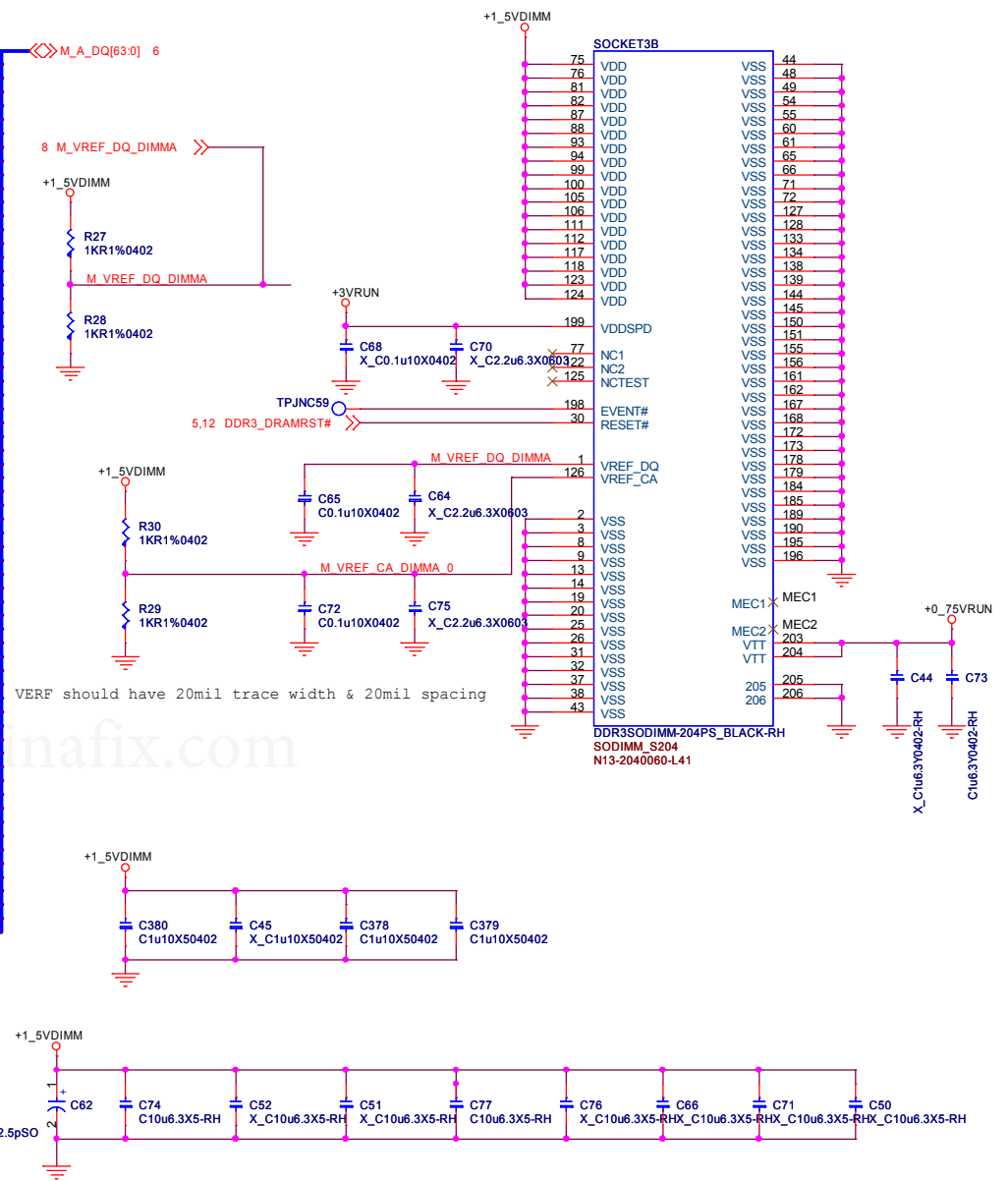
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled  01:Reserved--(device 1 functions 1 disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable


# SODIMM #A0

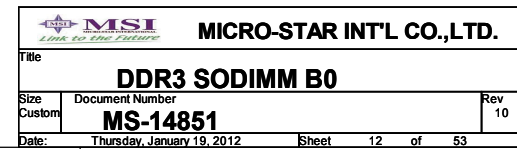


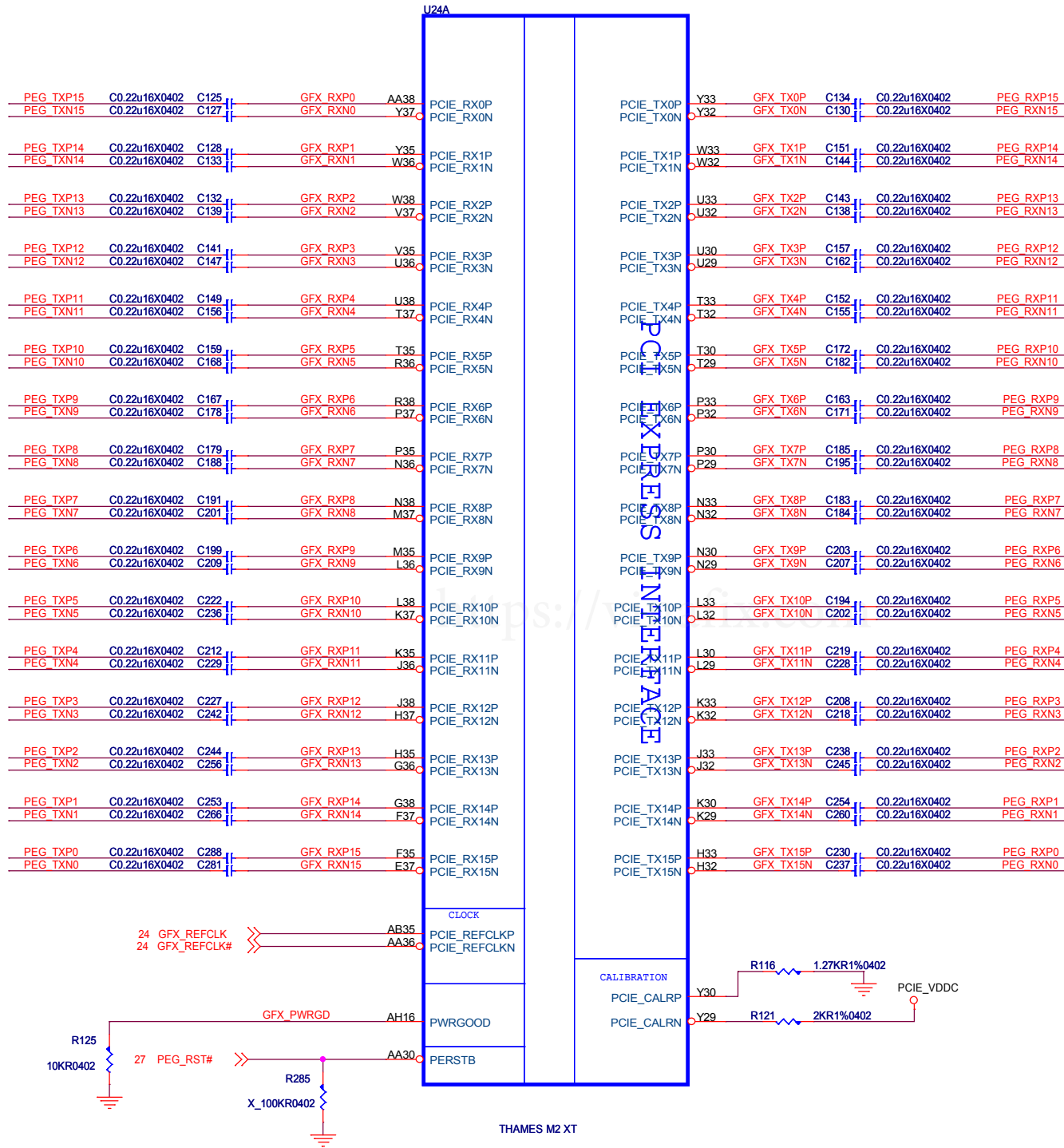
DDR3SODIMM-204PS\_BLACK-RH  
SODIMM\_S204  
N13-2040060-L41



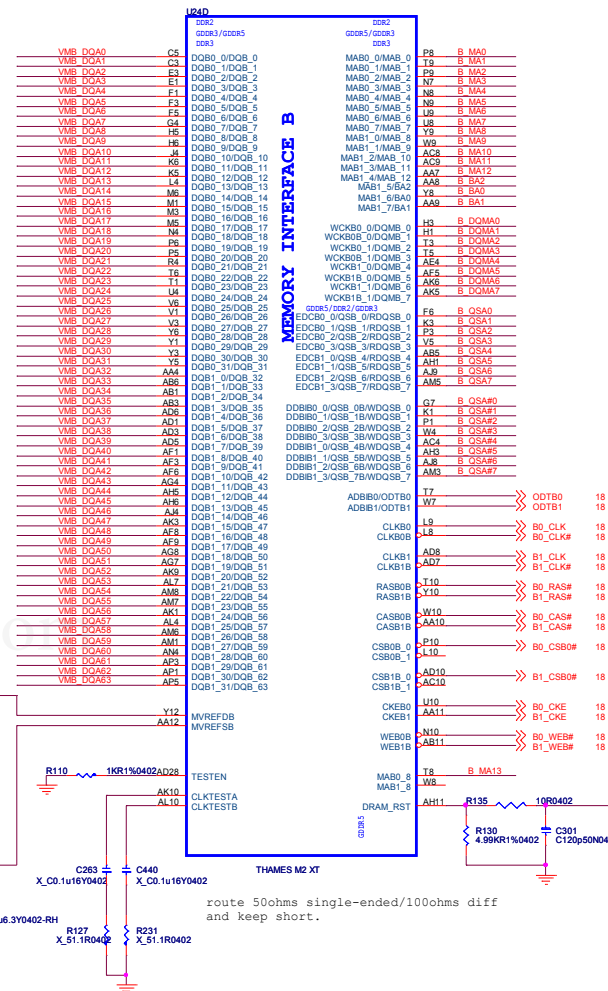
VERF should have 20mil trace width & 20mil spacing

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>DDR3 SODIMM A0</b>	
Size	Document Number
Custom	<b>MS-14851</b>
Date:	Thursday, January 19, 2012
Sheet	11 of 53
Rev	10





PEG\_RXN[15:0] 5  
PEG\_RXP[15:0] 5  
PEG\_TXN[15:0] 5  
PEG\_TXP[15:0] 5

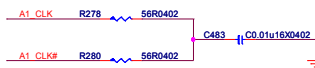
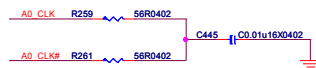
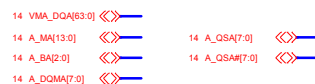
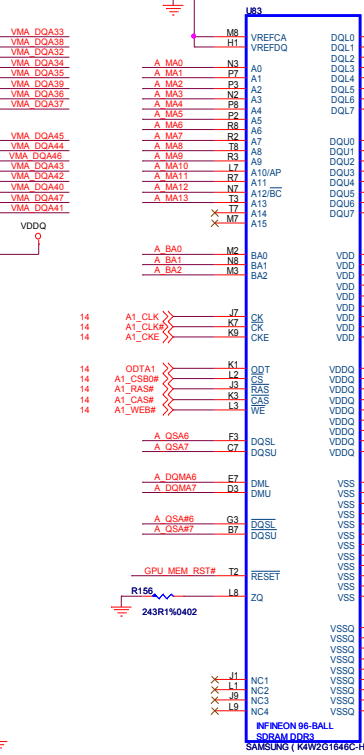
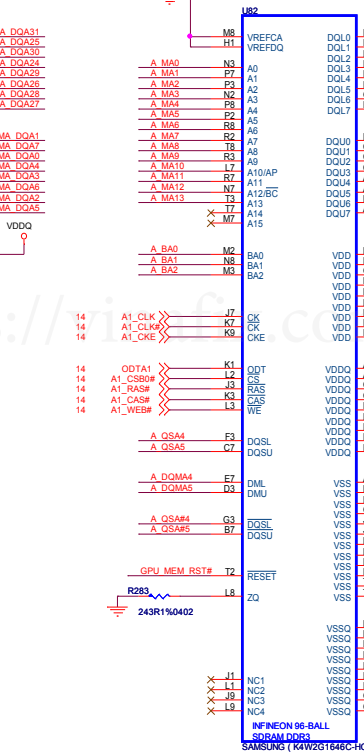
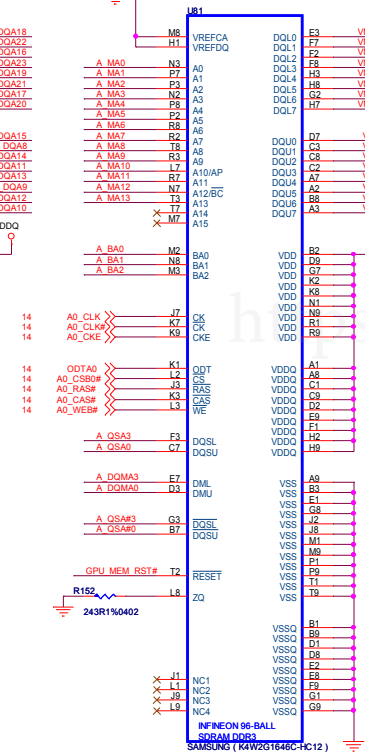
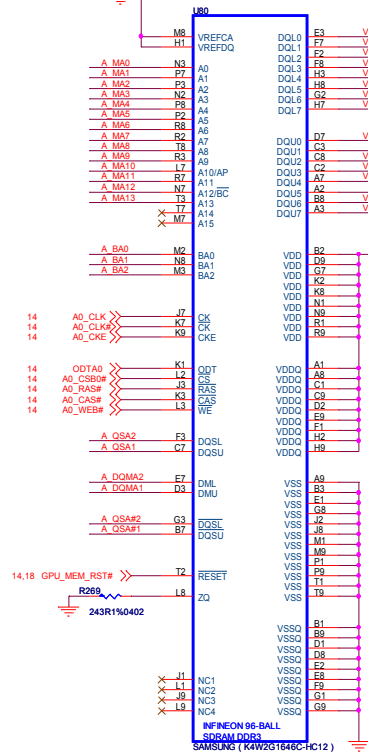
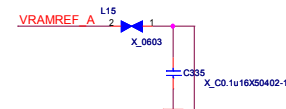
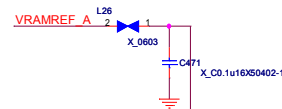
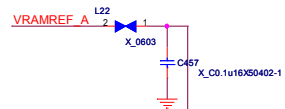
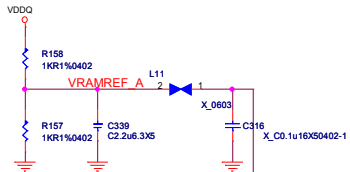
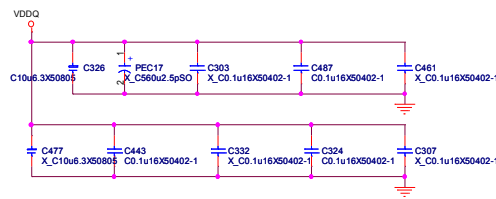
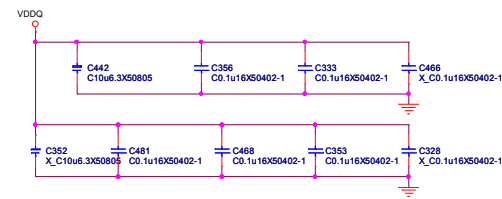


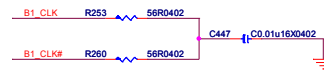
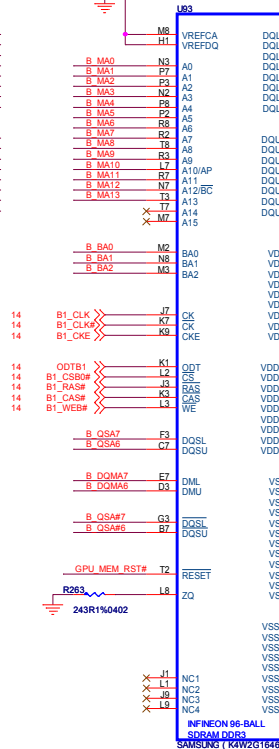
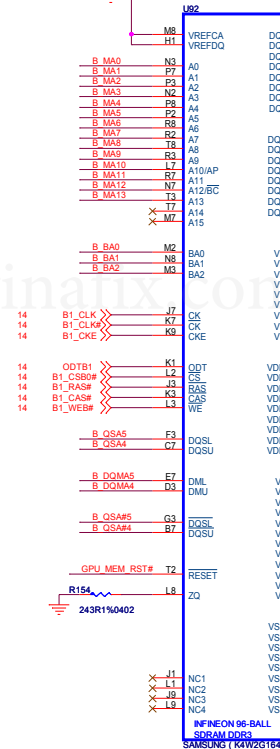
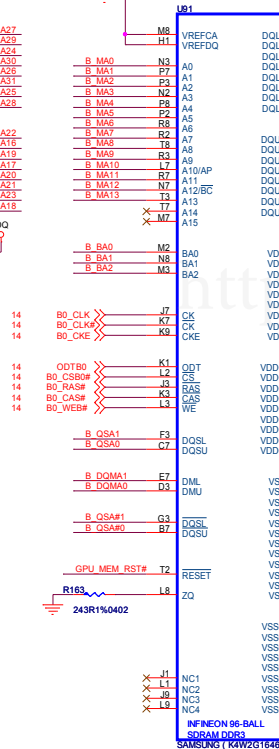
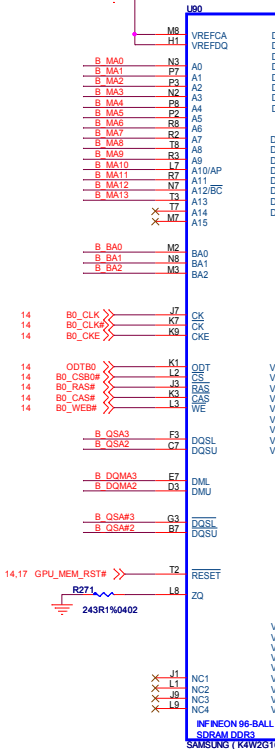
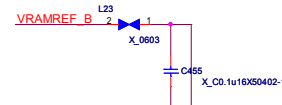
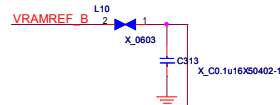
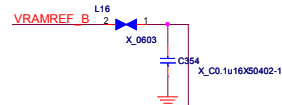
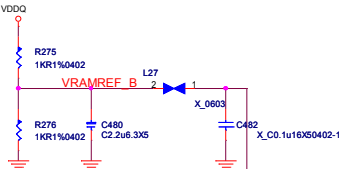
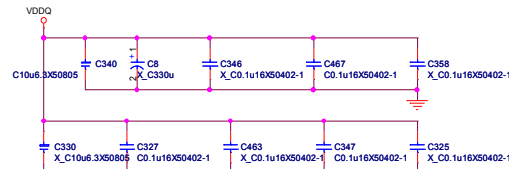
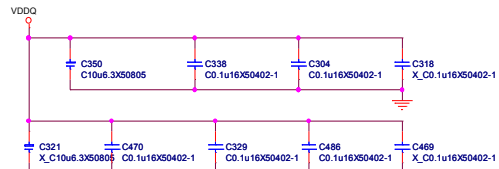


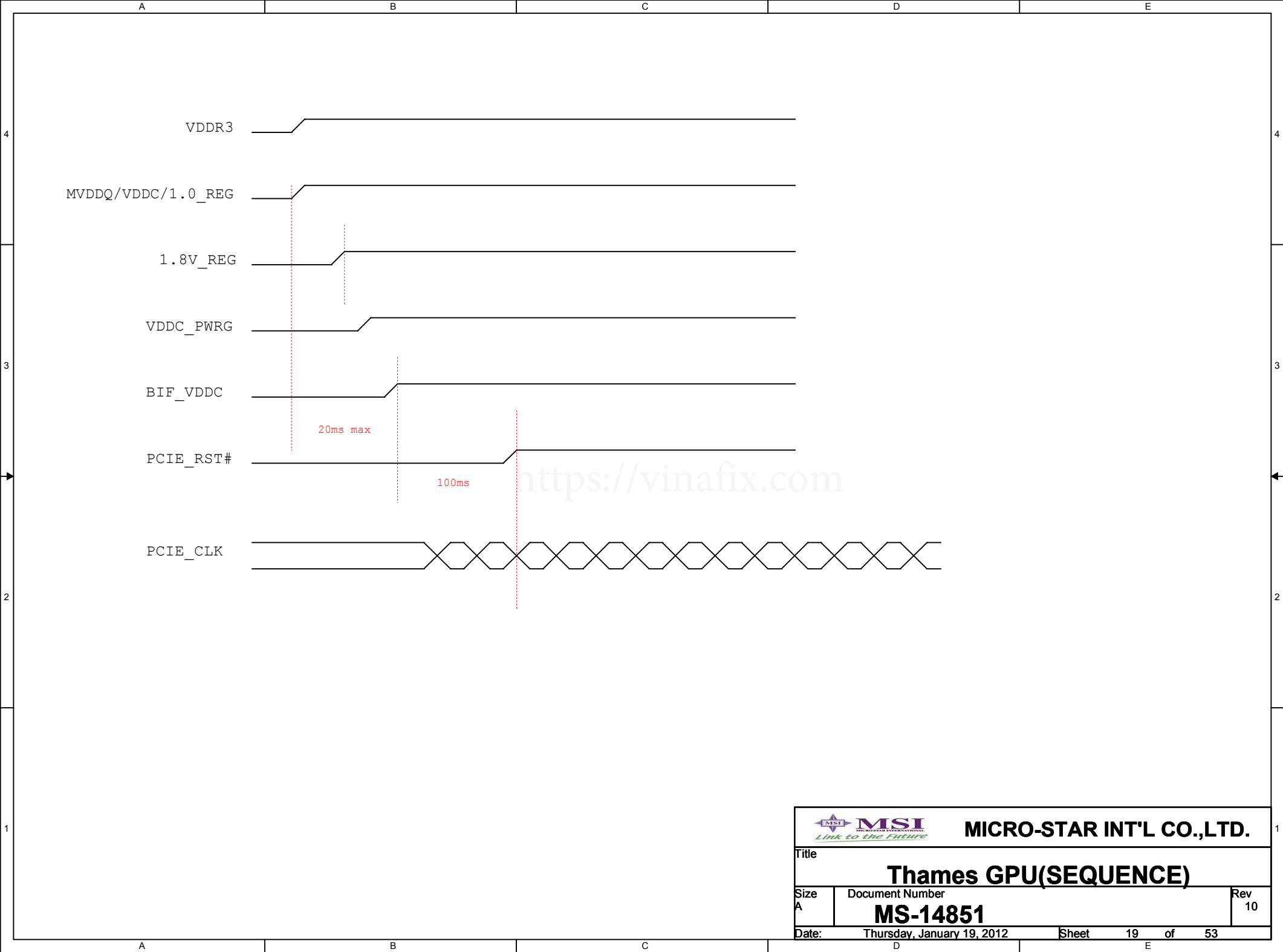


[illegible]

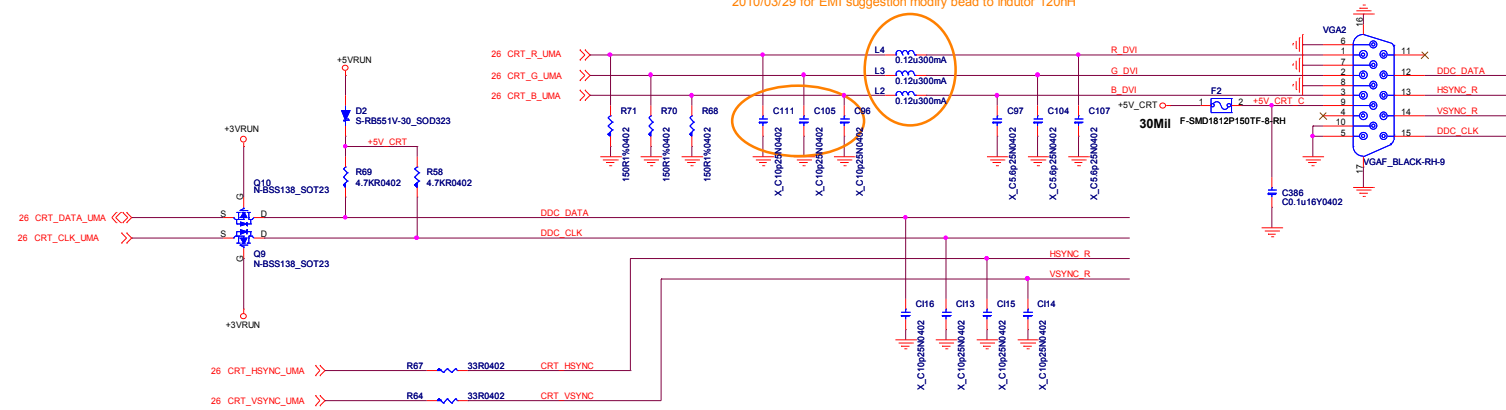




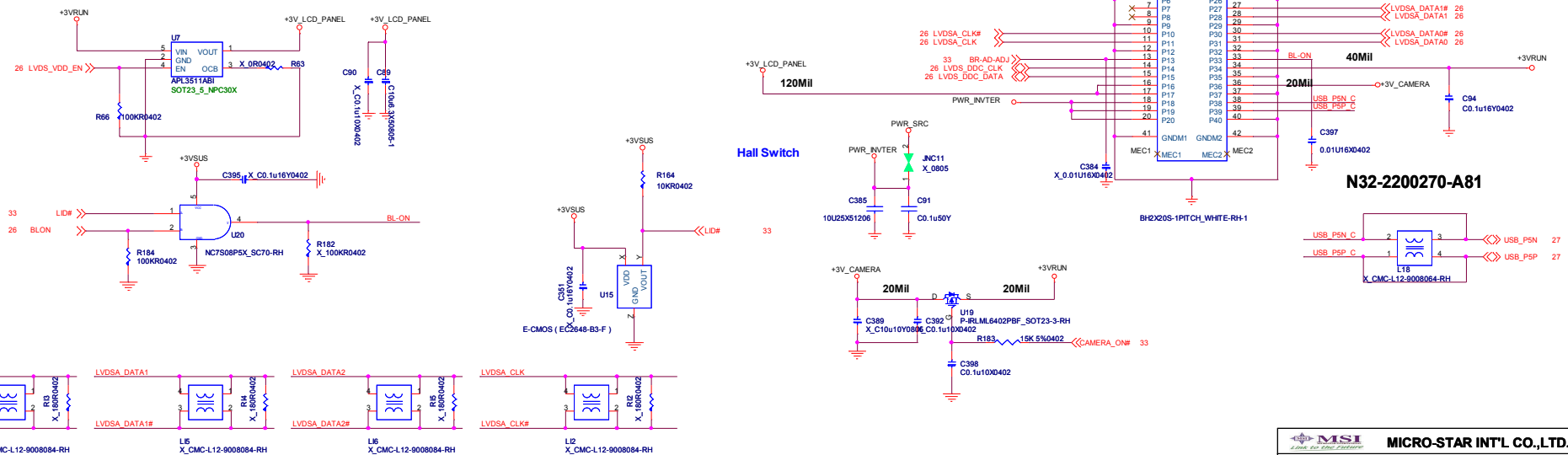


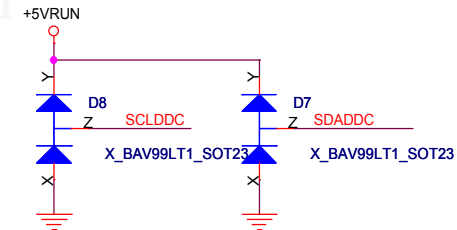
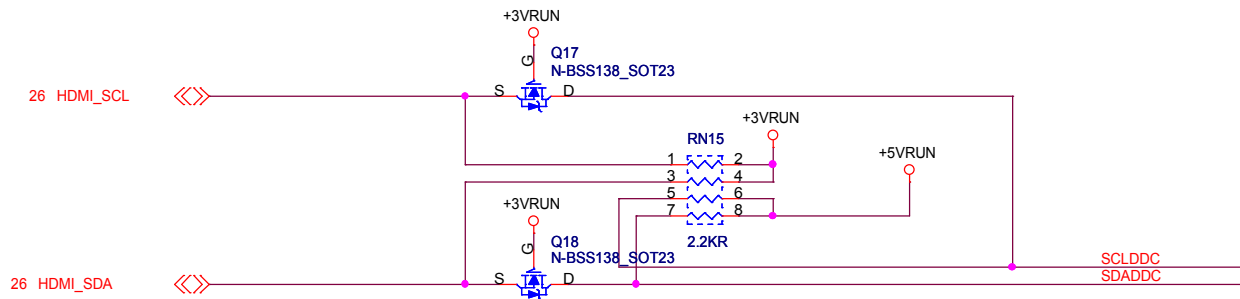
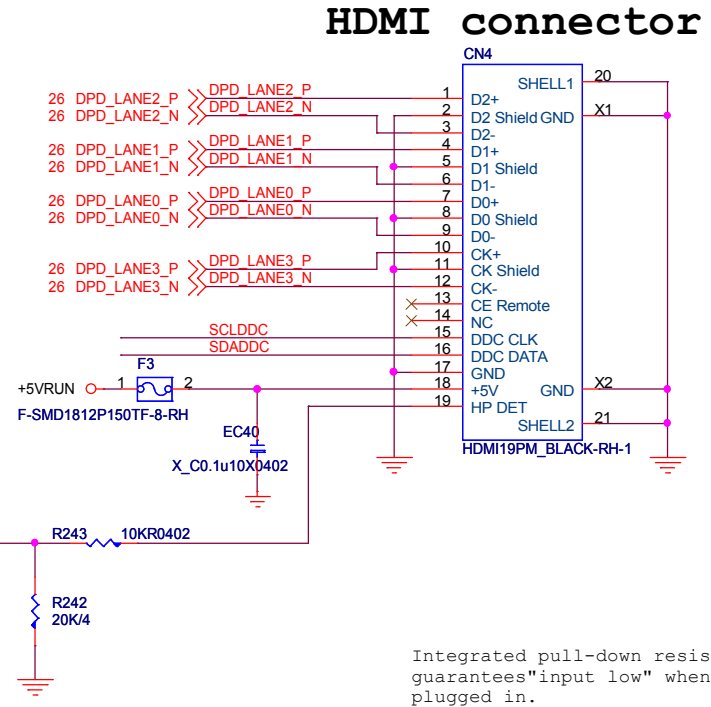
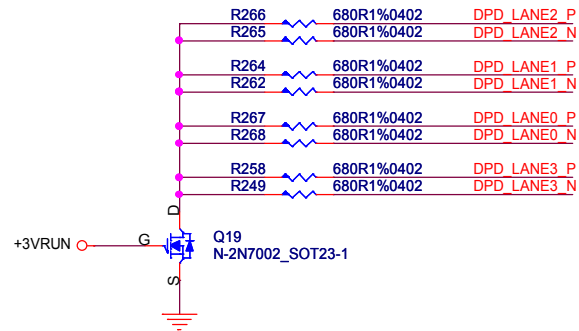



2010/03/29 for EMI suggestion modify bead to indutor 120nH

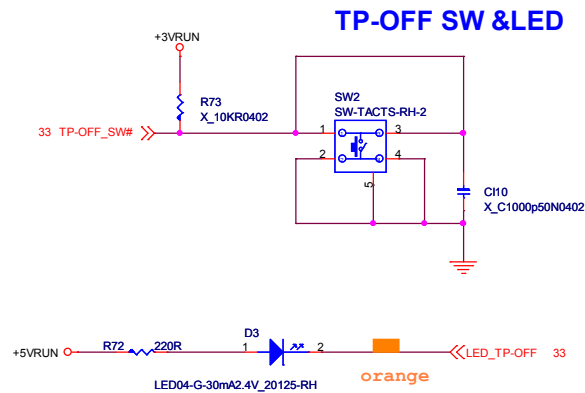
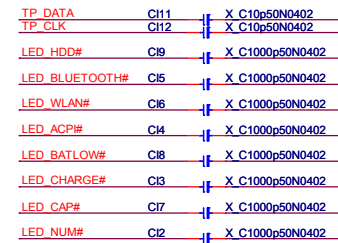
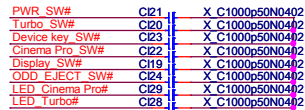


## LVDS

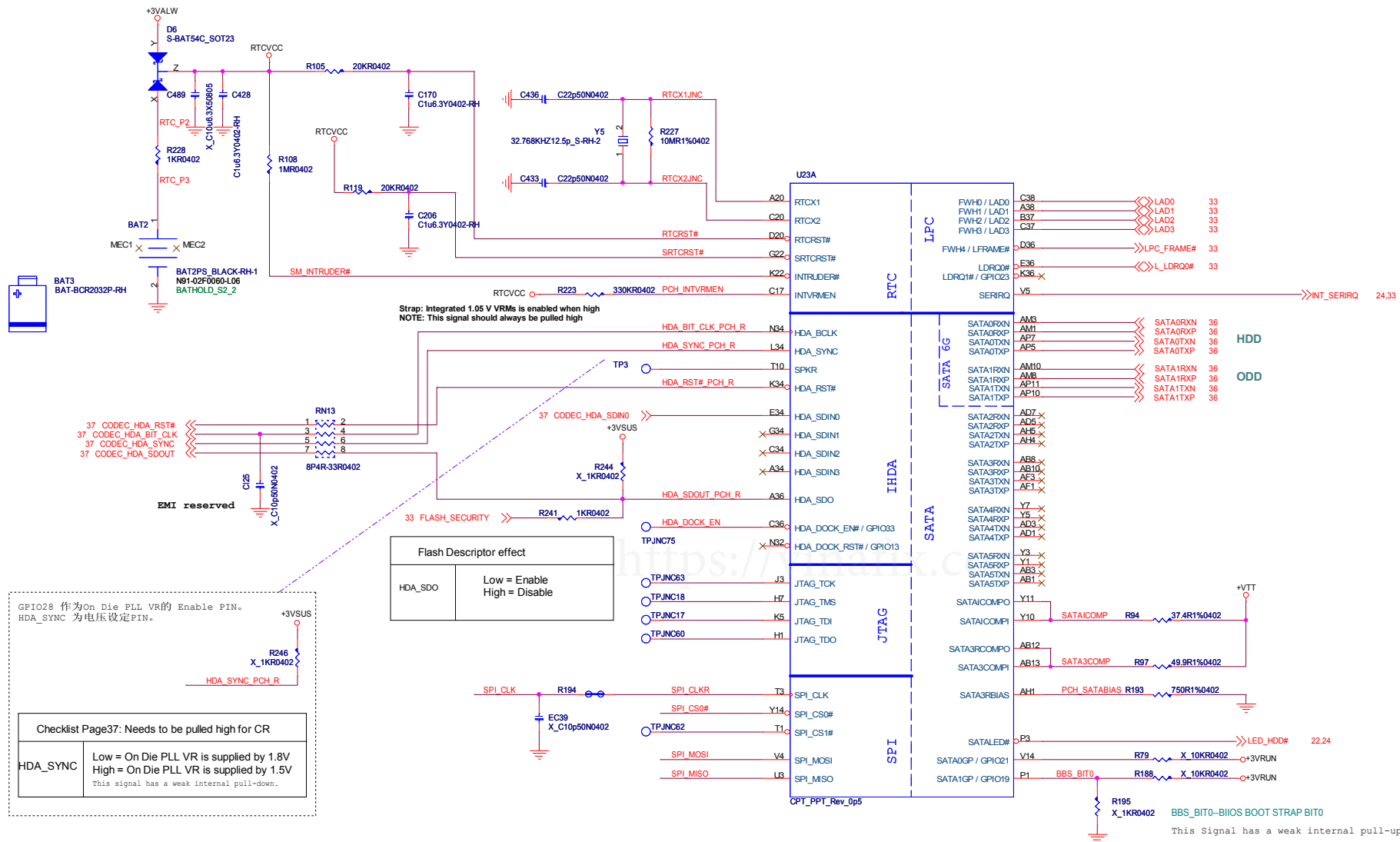




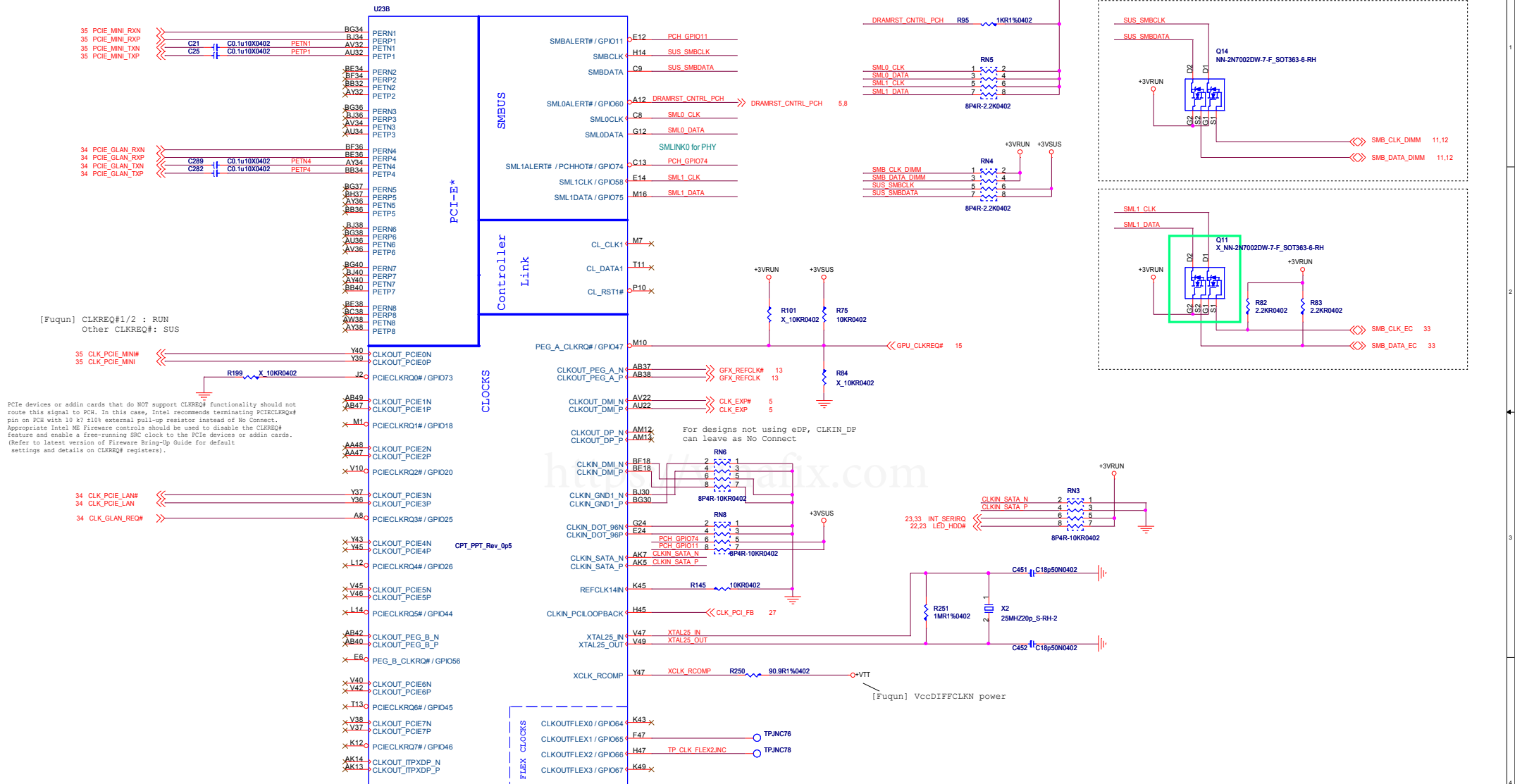
 <b>MICRO-STAR INT'L CO.,LTD.</b>		
Title		
<b>HDMI</b>		
Size	Document Number	Rev
Custom	<b>MS-14851</b>	10
Date:	Thursday, January 19, 2012	Sheet 21 of 53



# PANTHER POINT (HDA, JTAG, SATA)



## PANTHER POINT (PCI-E, SMBUS, CLK)



Intel Comments:

If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.

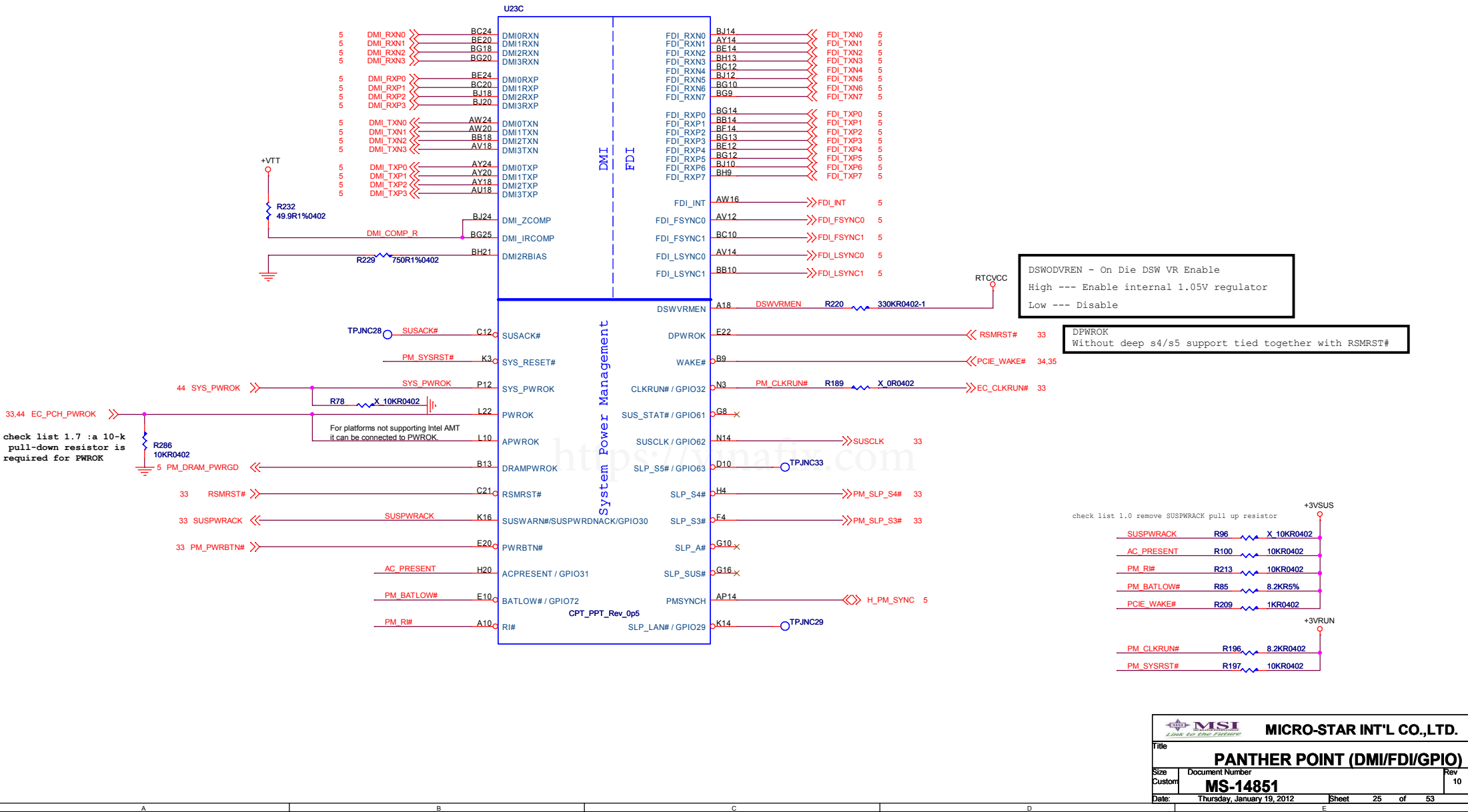
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.

Intel recommends terminating PCIECLKREQ# pin on PCH with 10 k  $\pm$ 10% external pull-up resistor instead of

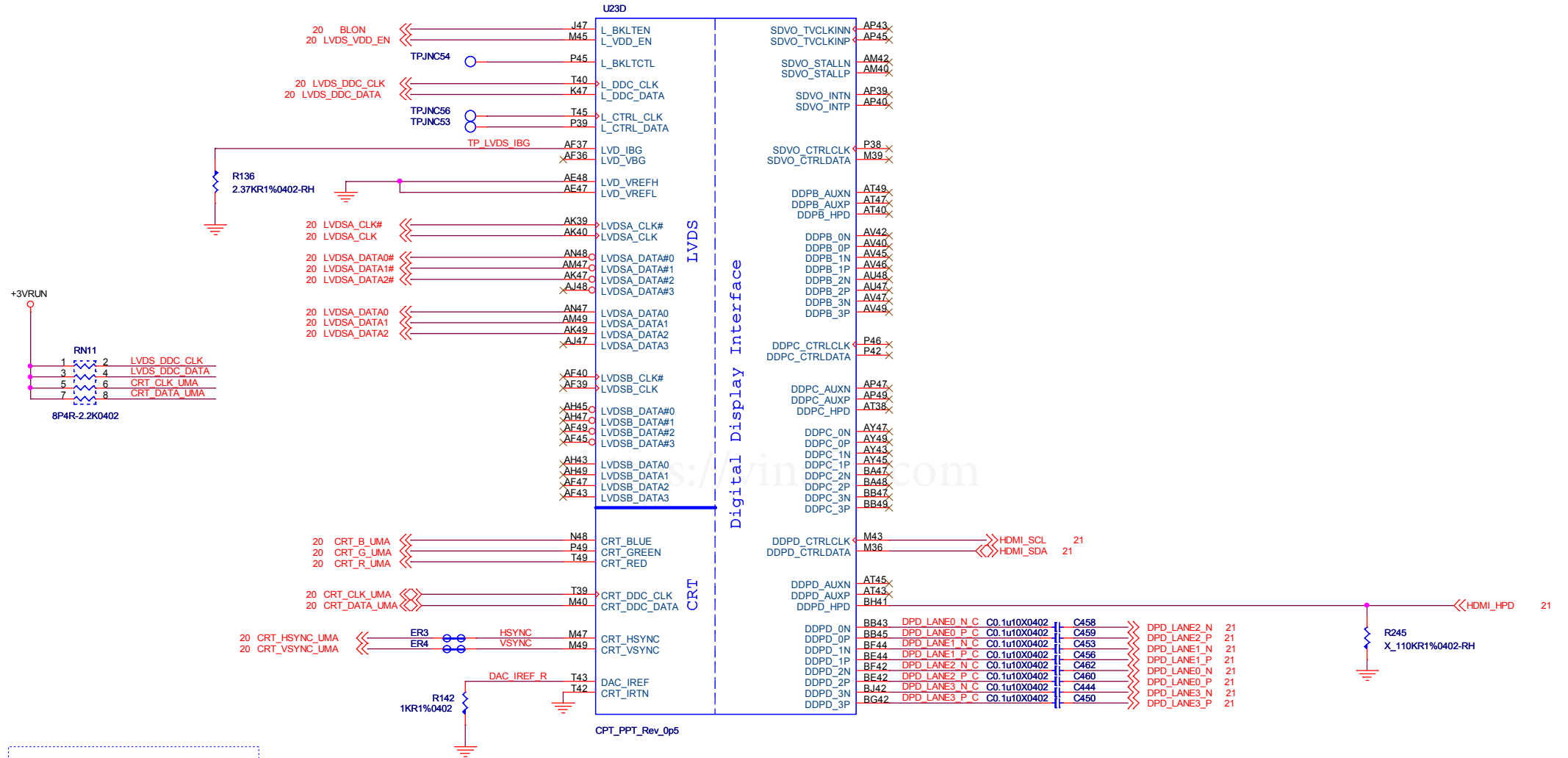
~~DRGPIO[2:1]#~~ on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.



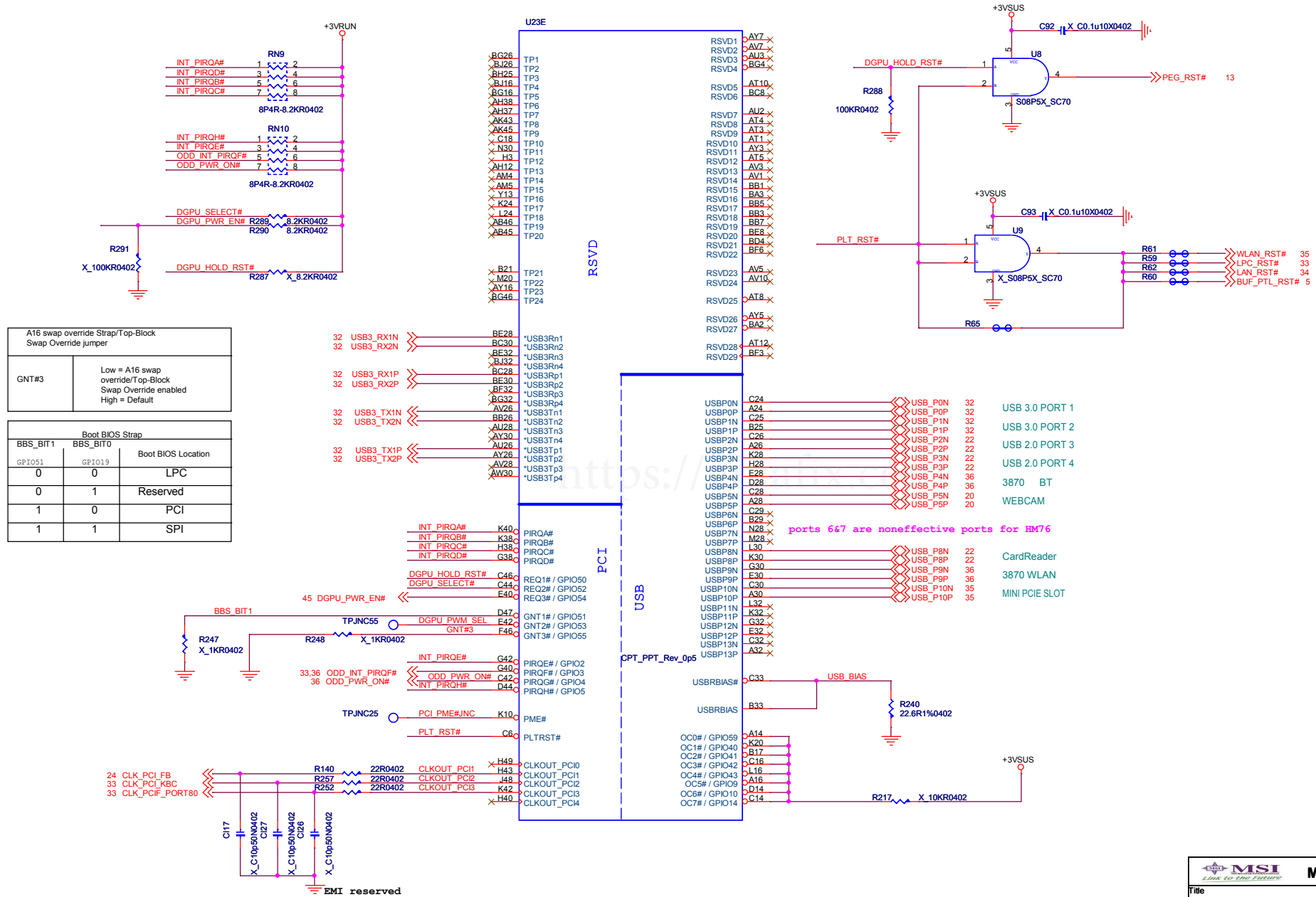
PANTHER POINT (DMI, FDI, GPIO)



# PANTHER POINT (LVDS,DDI)



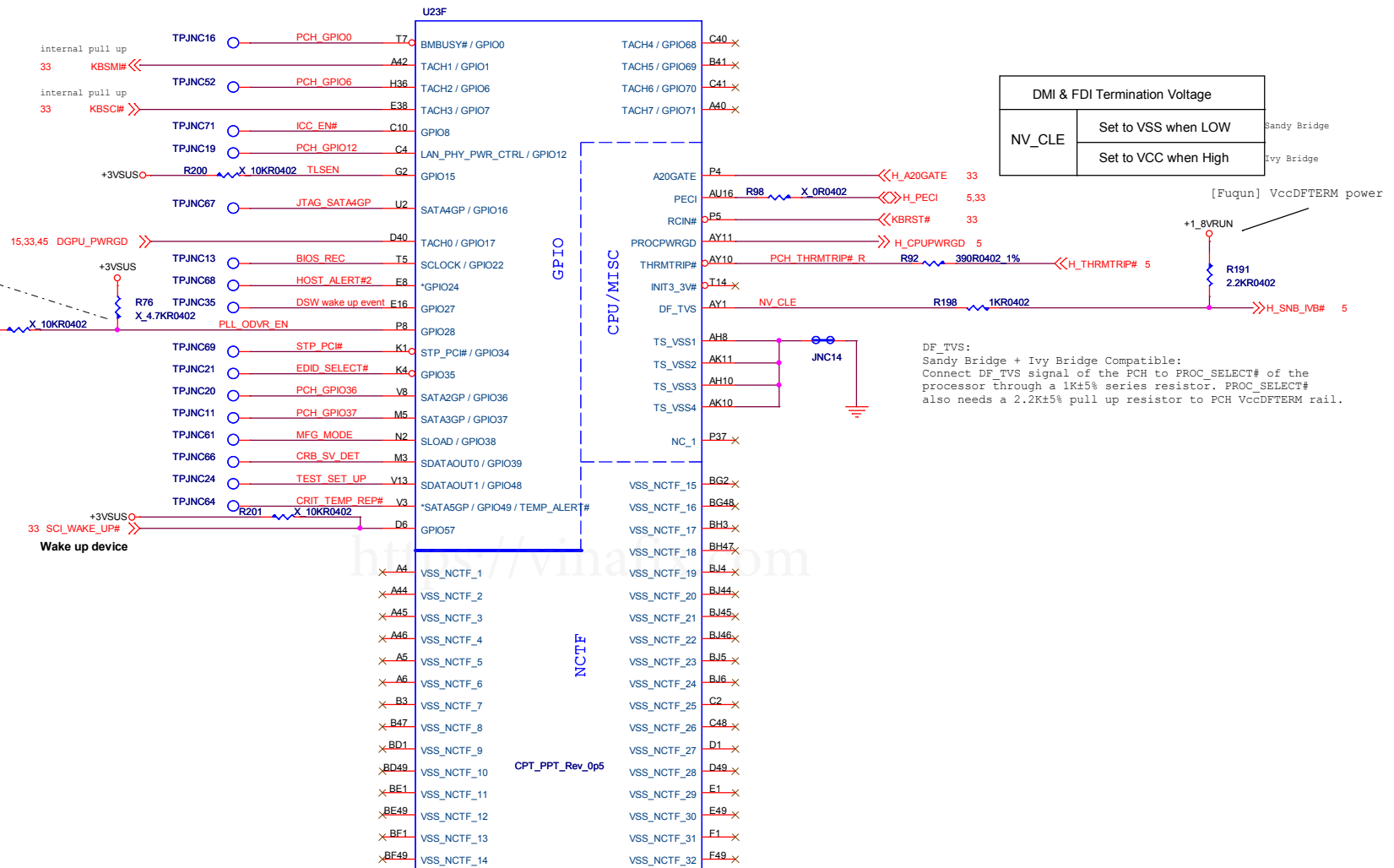
## PANTHER POINT (PCI,USB,NVRAM)




# PANTHER POINT (GPIO,VSS\_NCTF,RSVD)

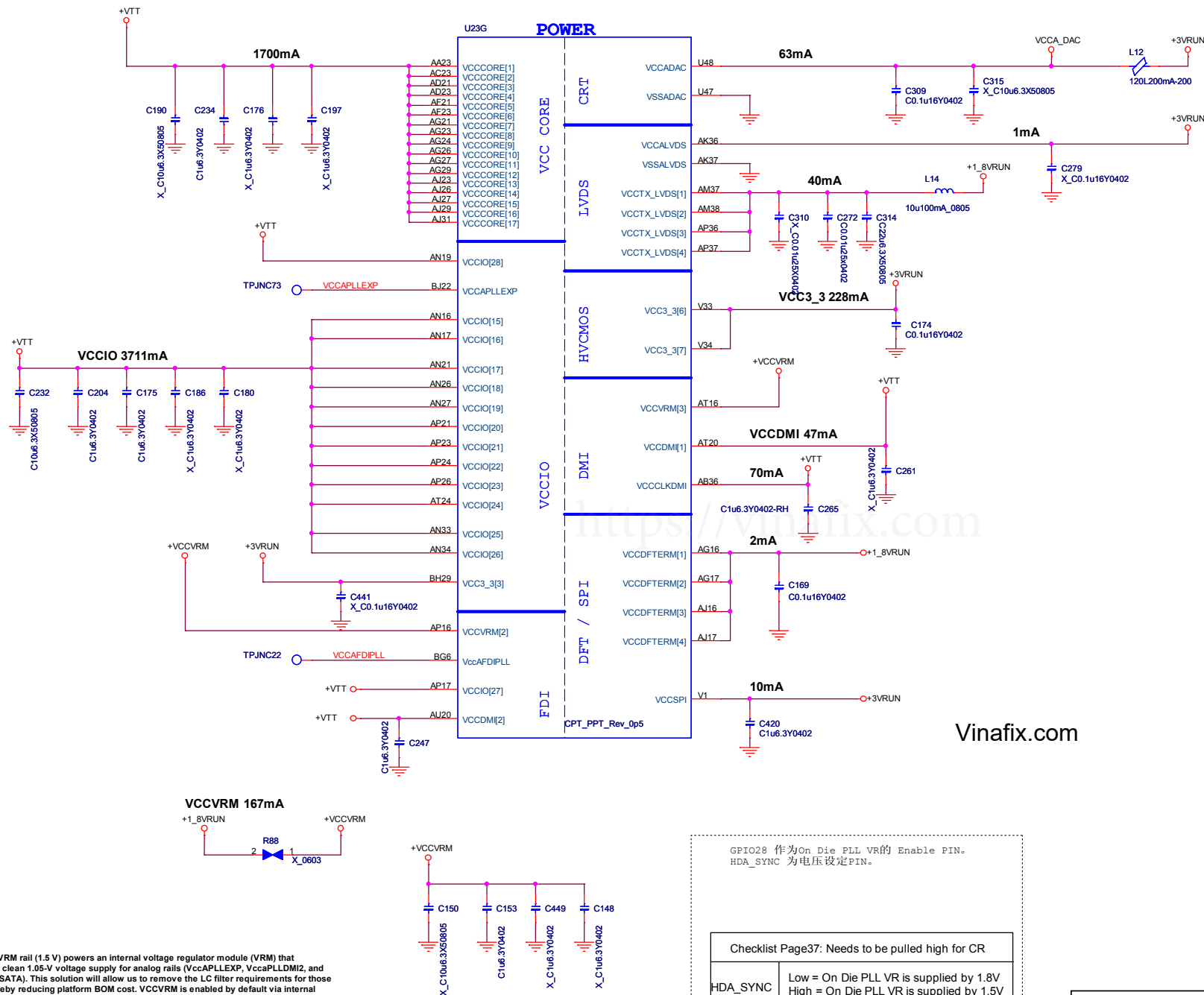
PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

when use as the chipset test interface,GPIO28 signal needs to be pulled up to 3.3V\_SUS with 4.7K resistor to ensure proper strap setting



 <b>MSI</b> <i>A Look for Your Future</i>		<b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>PANTHER POI (GPIO/NCTF/RSVD)</b>			
<b>Size</b> Custom	<b>Document Number</b> <b>MS-14851</b>		<b>Rev</b> 10
<b>Date:</b> Thursday, January 19, 2012	<b>Sheet</b> 28 of 53		

# PANTHER POINT (POWER)



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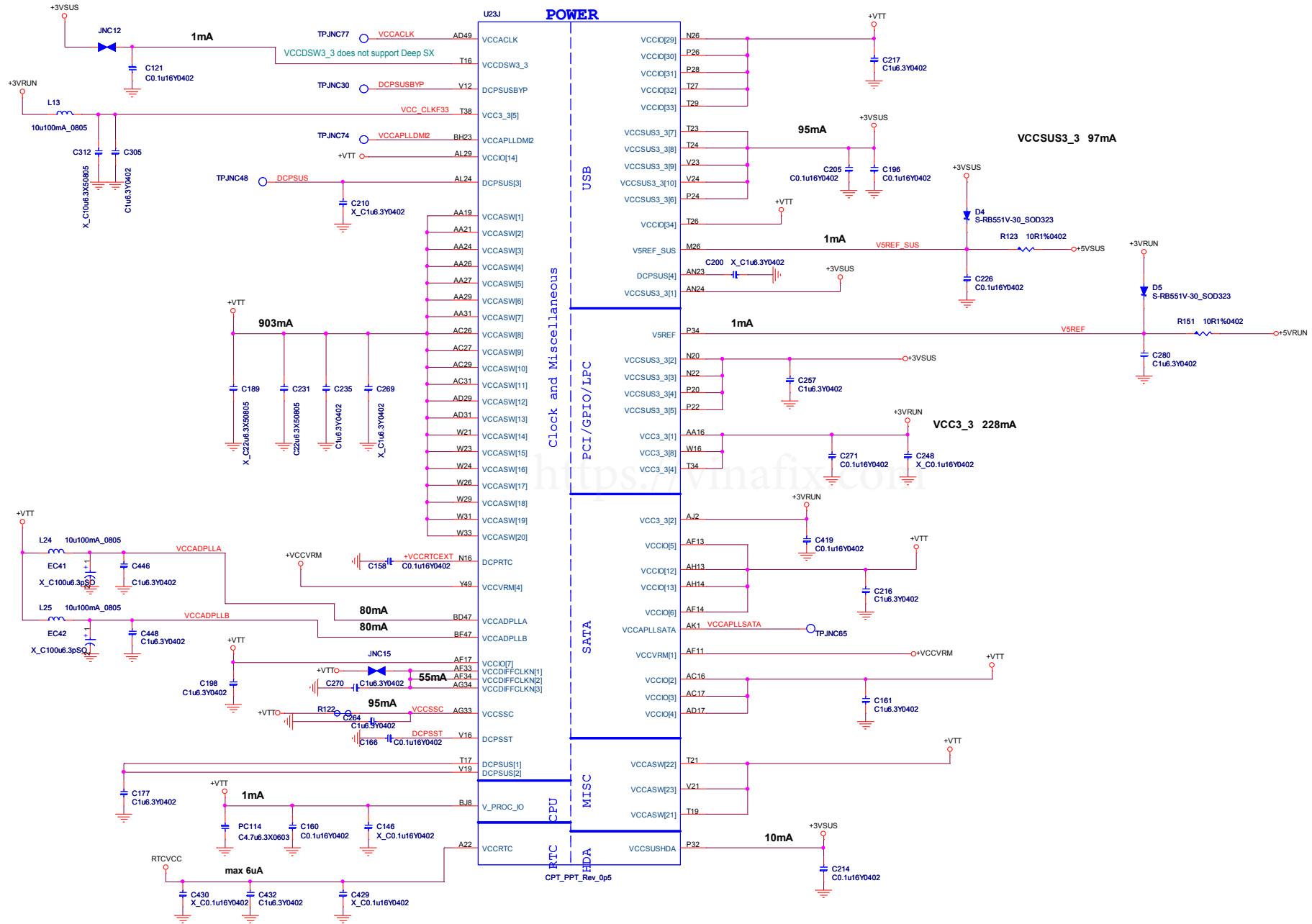
GPIO28 作为 On Die PLL VR 的 Enable PIN.  
HDA\_SYNC 为电压设定 PIN.

Checklist Page37: Needs to be pulled high for CR

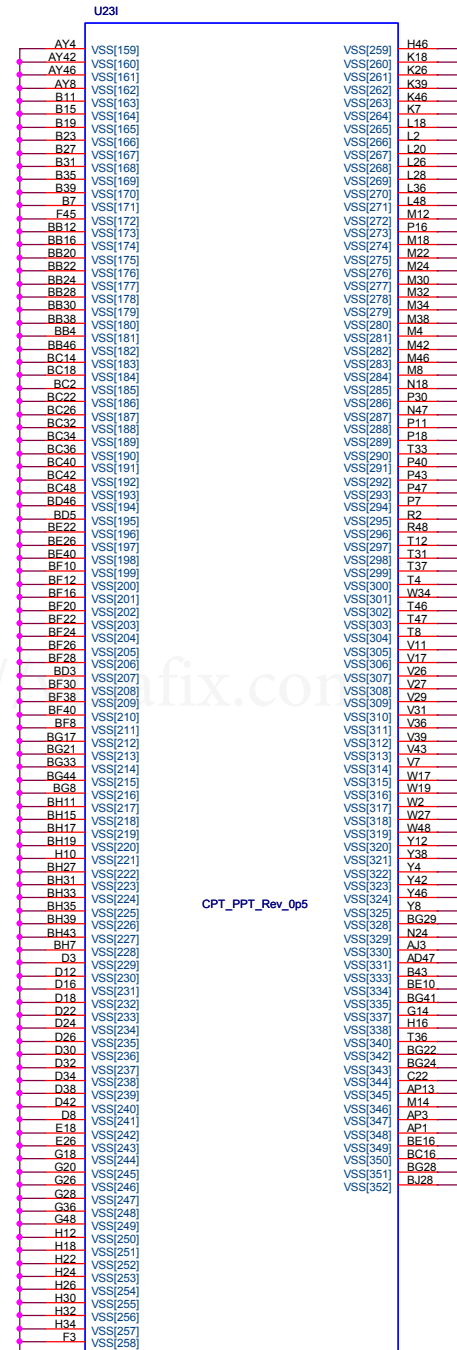
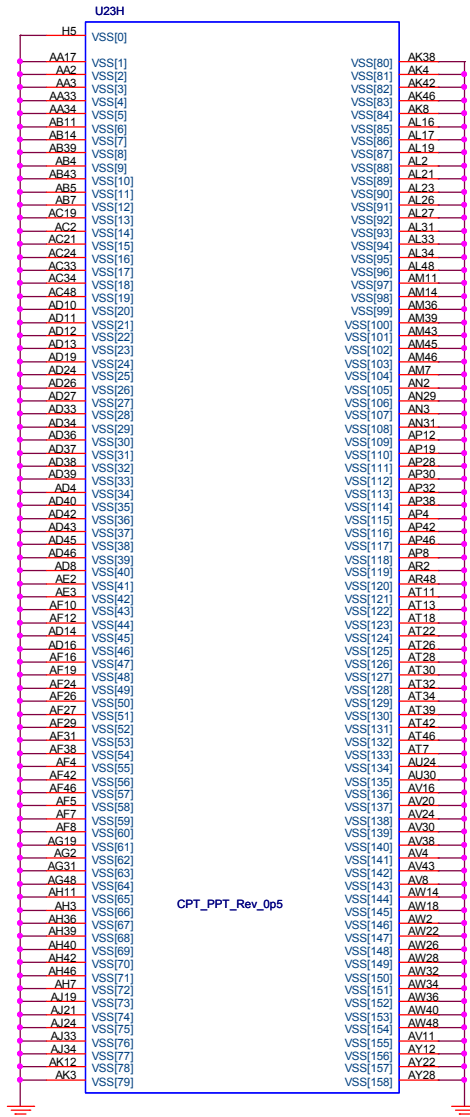
HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V This signal has a weak internal pull-down.
----------	---

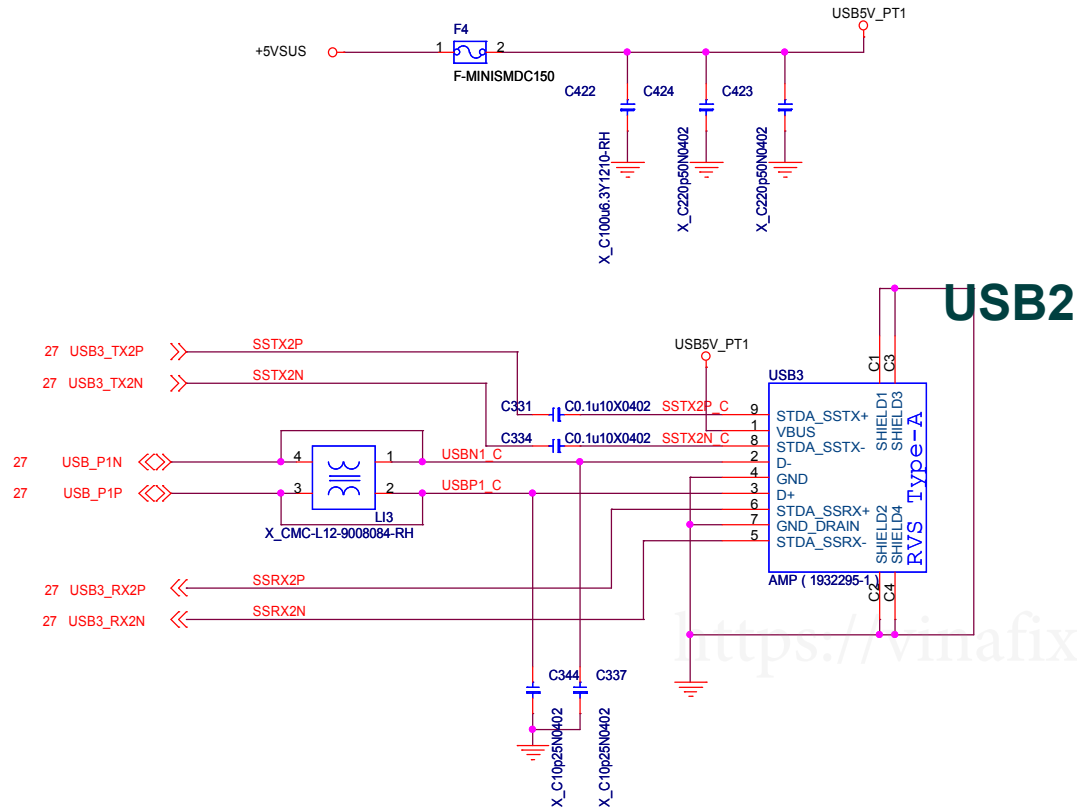
The VCCVRM rail (1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VccAPLLEX, VccAPLLDM2, and VccAPLLSATA). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO28.

## PANTHER POINT (POWER)

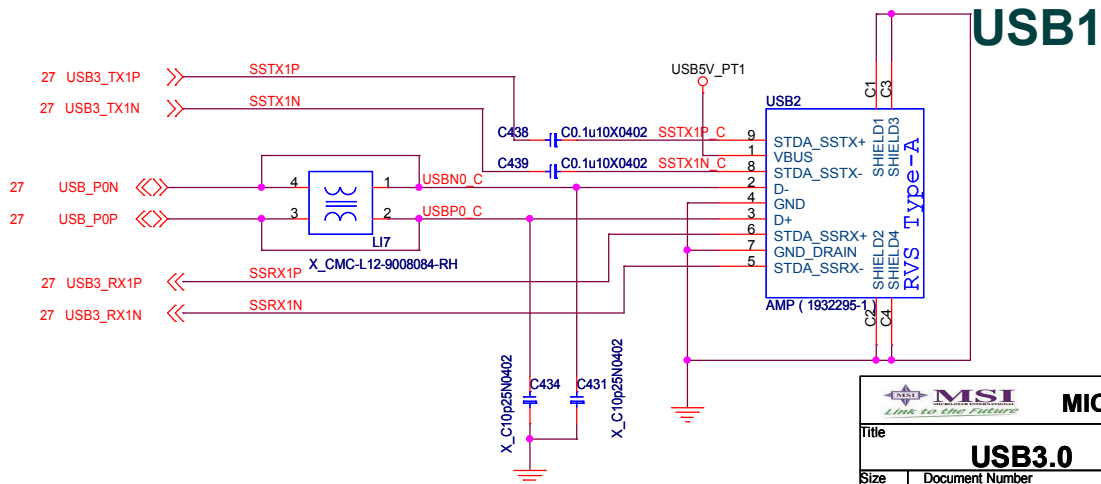


# PANTHER Point (GND)





USB2



USB1





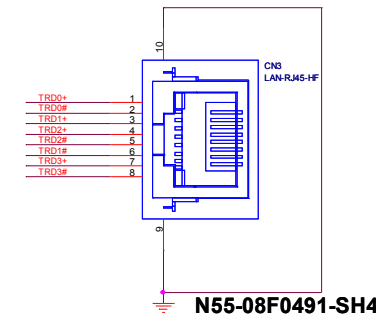
Use External 1.05V Supply When Disable Switch Regulator.  
If Using External 1.2V Supply Pls. Contact With FAE.

2010/01/08 remove it,If used jump write

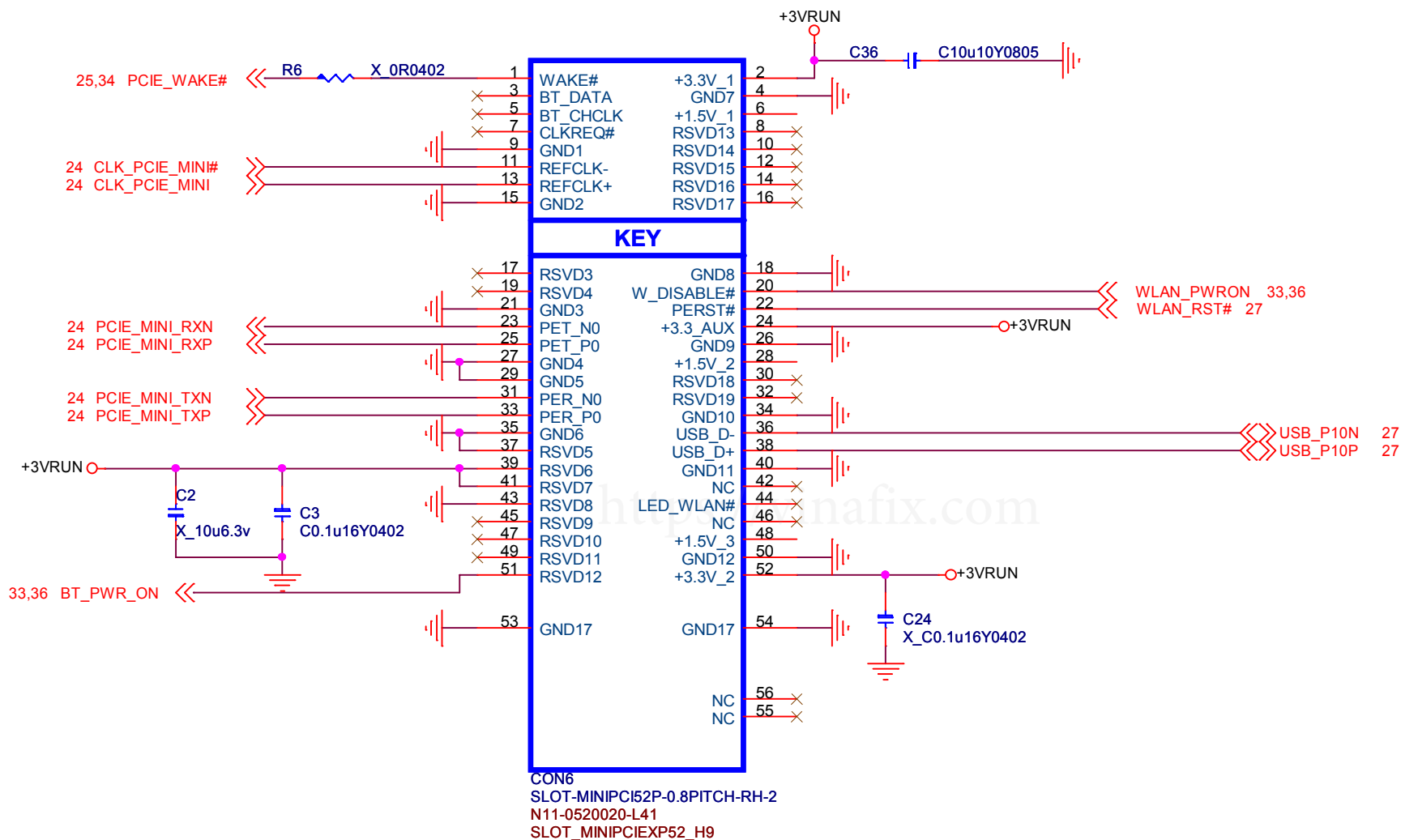


1E

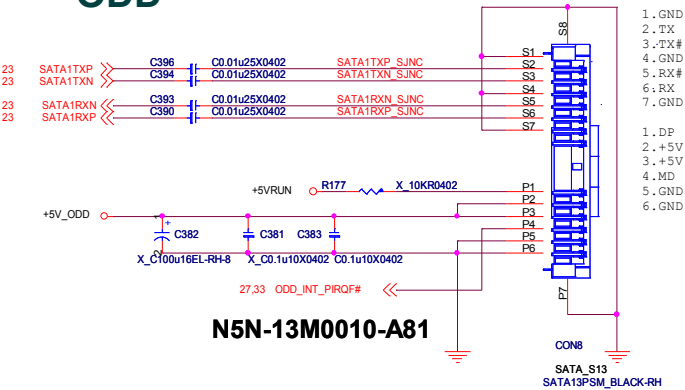
### 3. When using EFuse/BIOS Patch without ASF function.



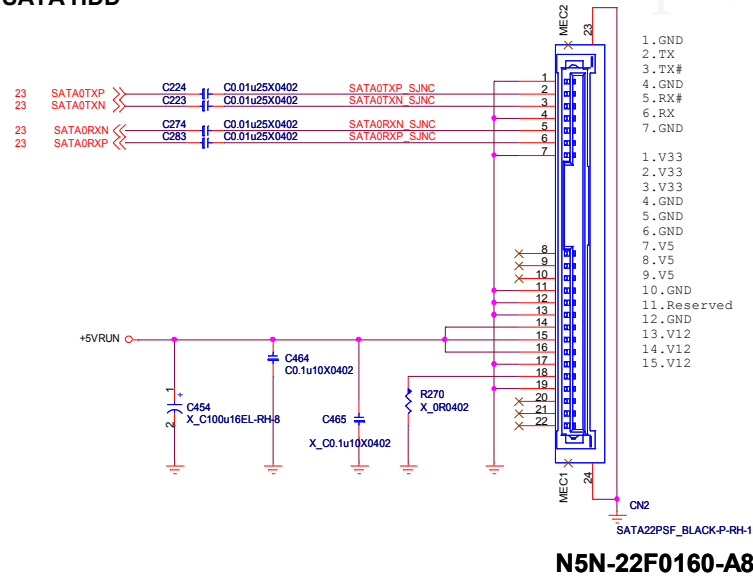
# WLAN



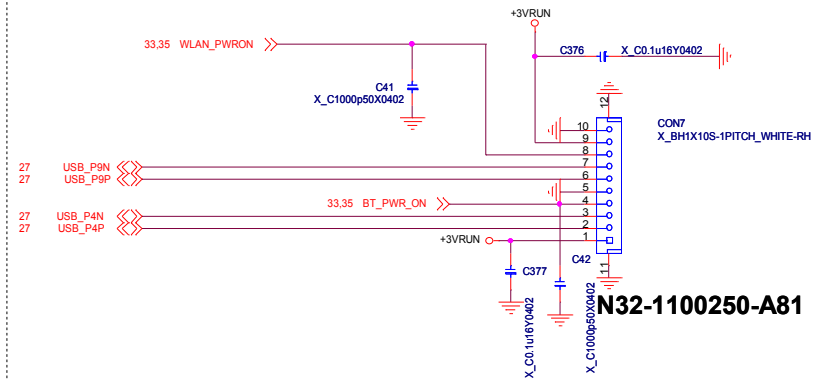
## ODD



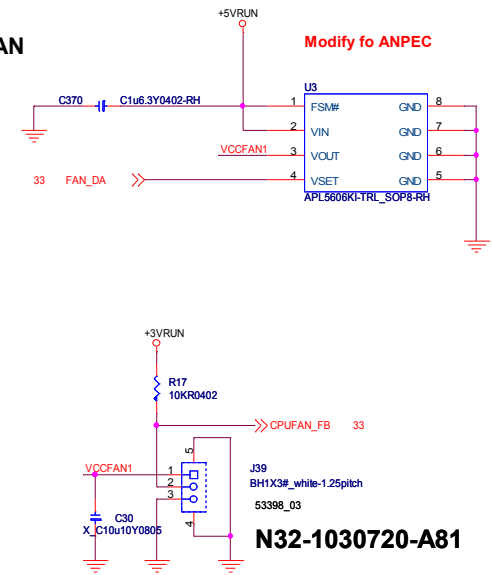
## SATA HDD

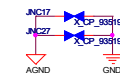
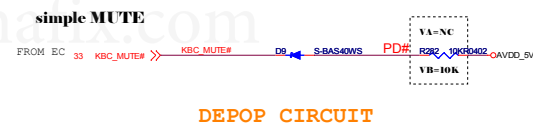
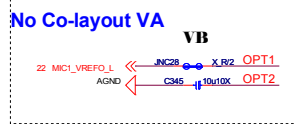


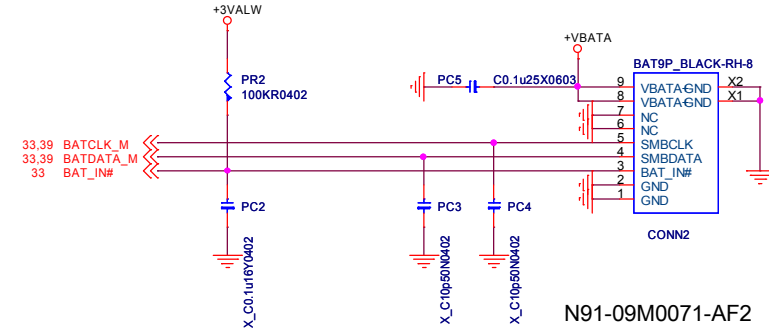
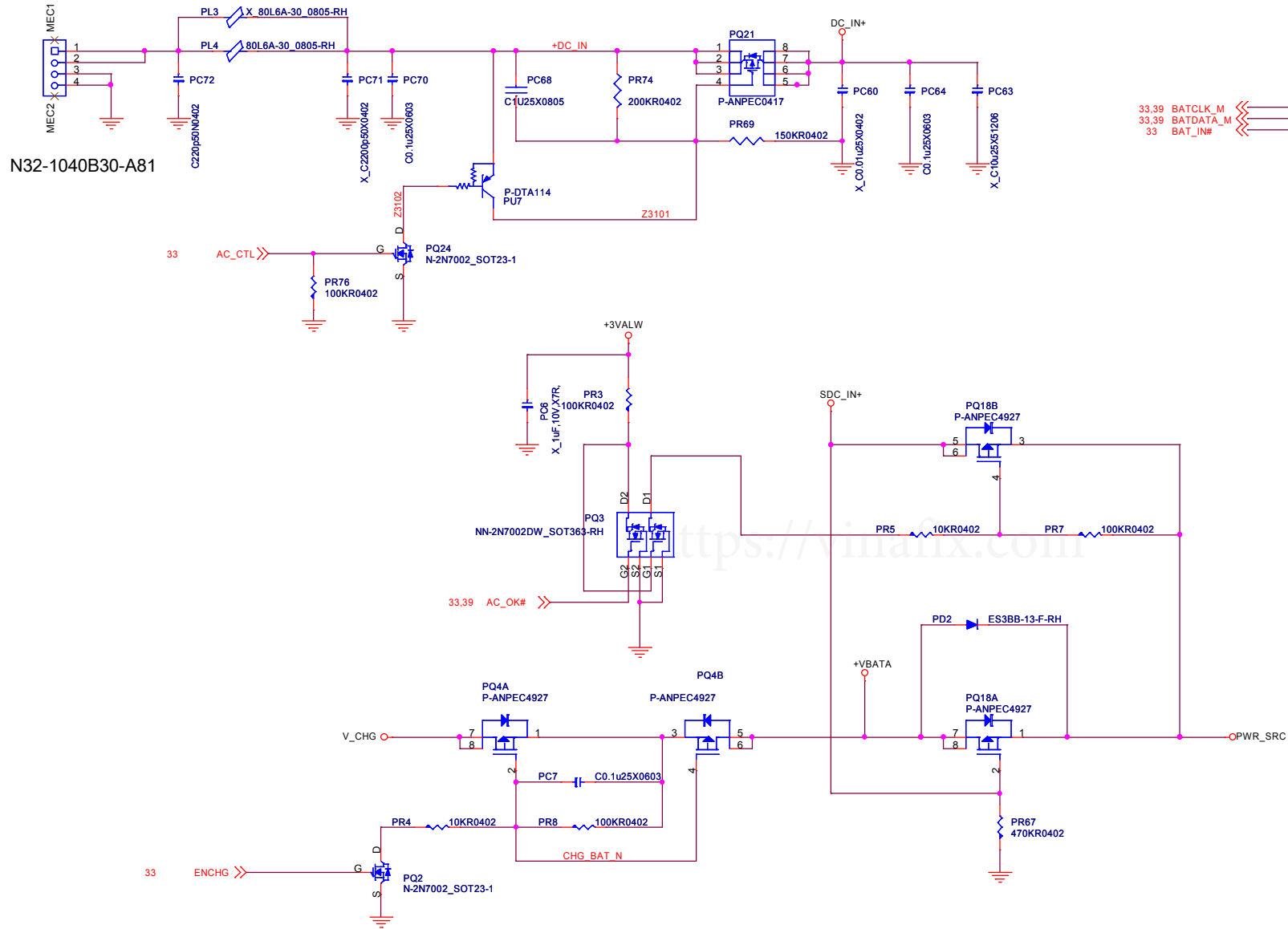
## WLAN/BT (3870)




## CPU FAN

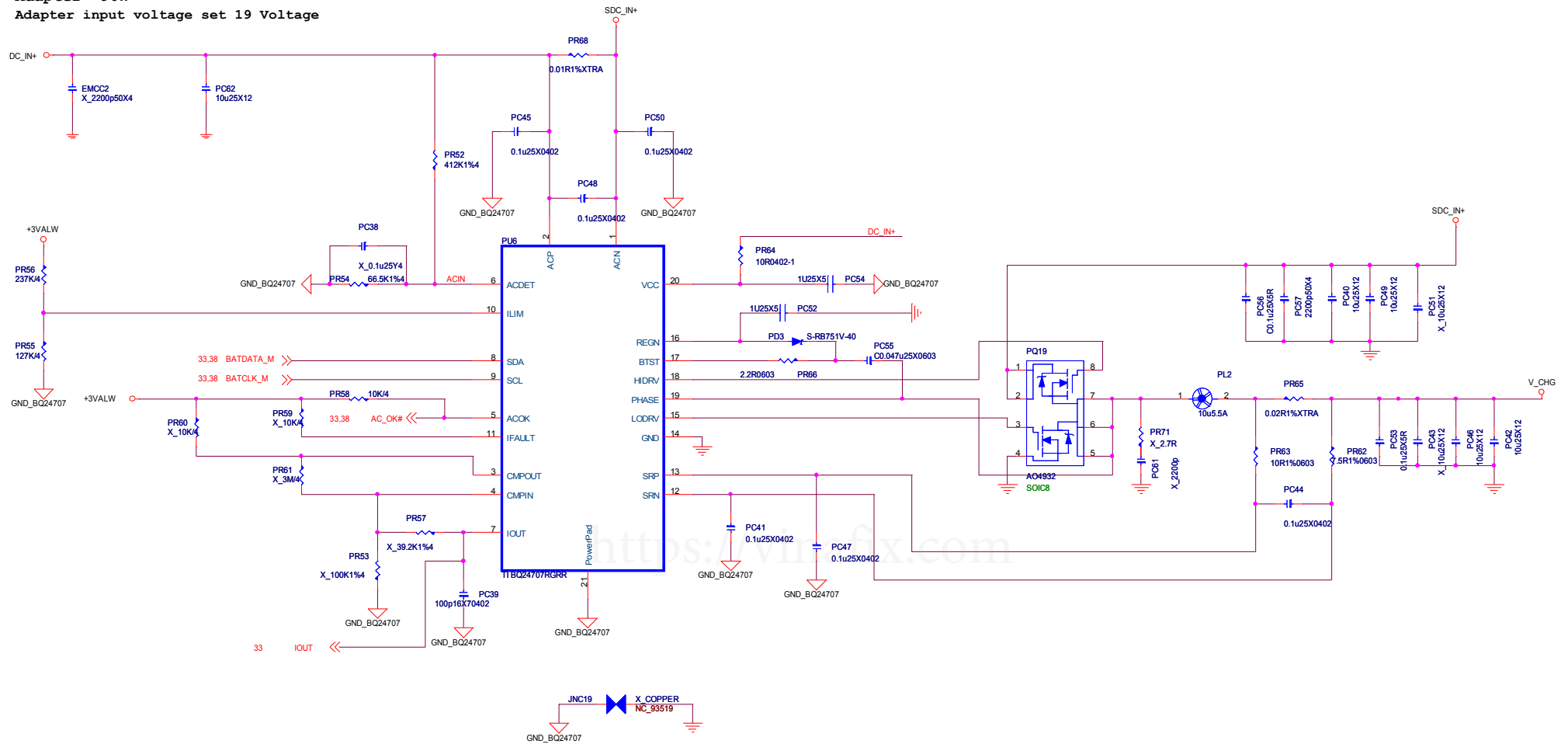






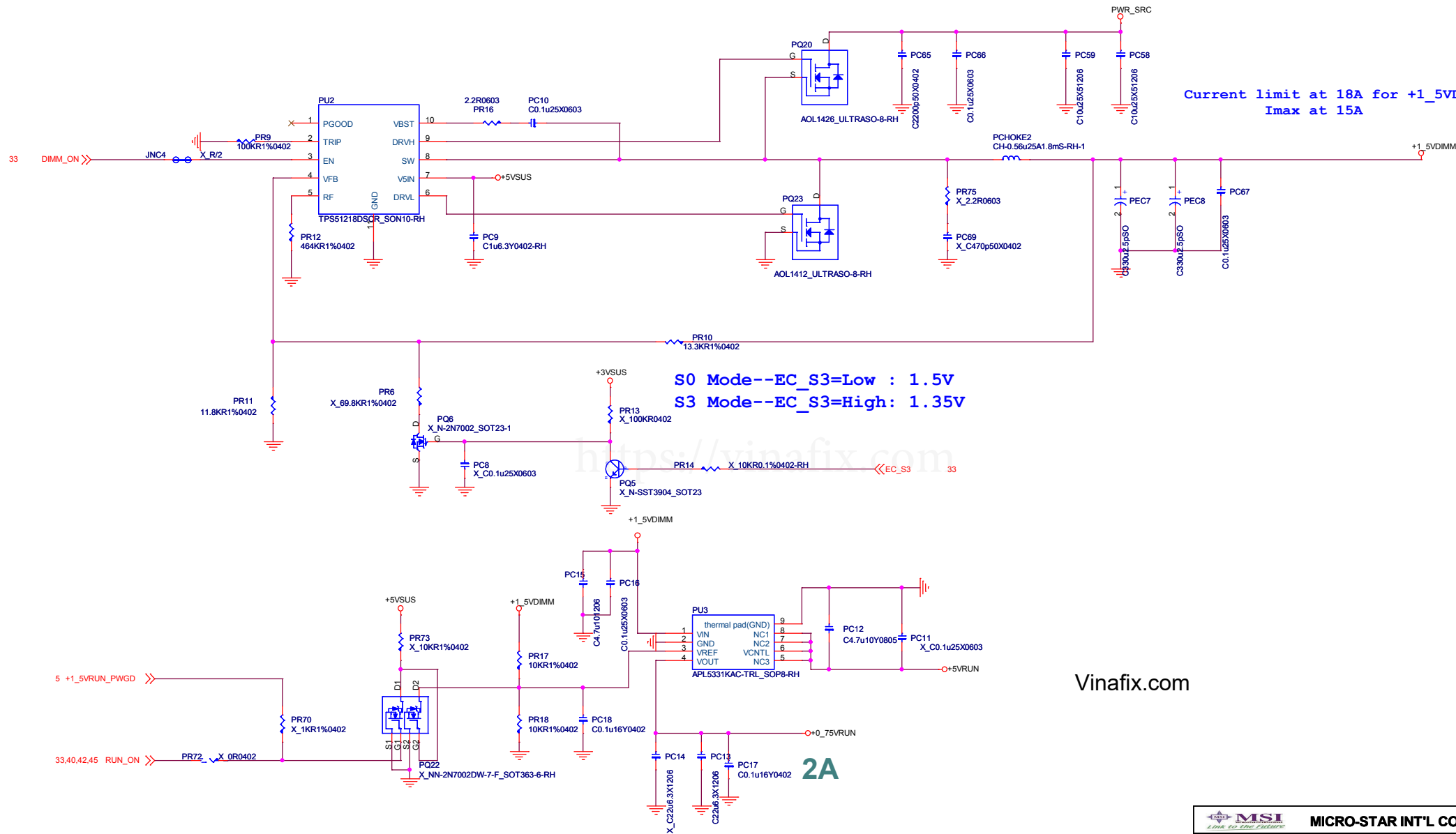
 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>Battery select</b>	
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Adapter= 90W  
Adapter input voltage set 19 Voltage




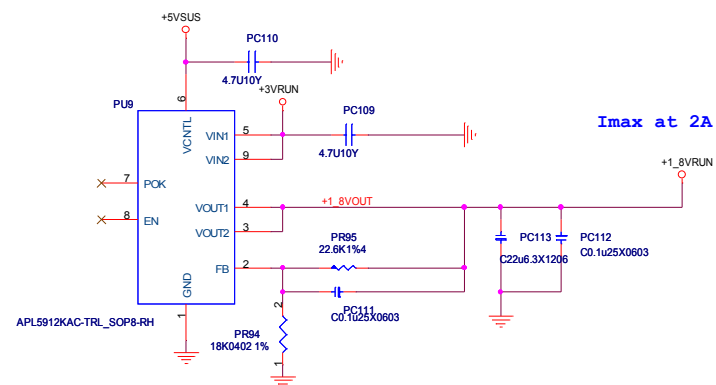
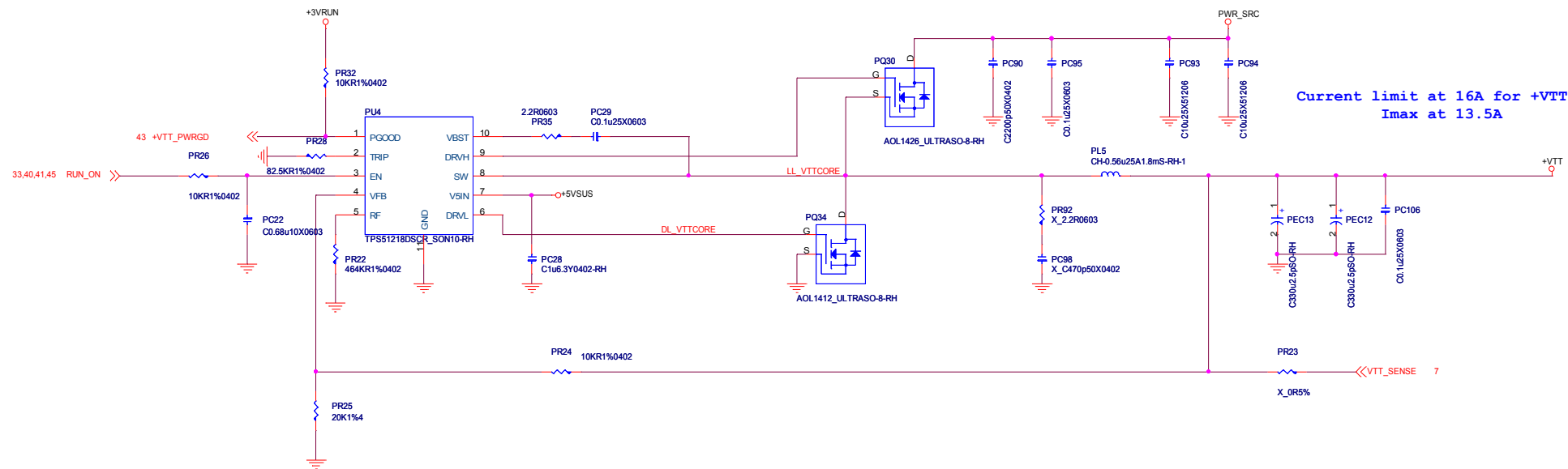




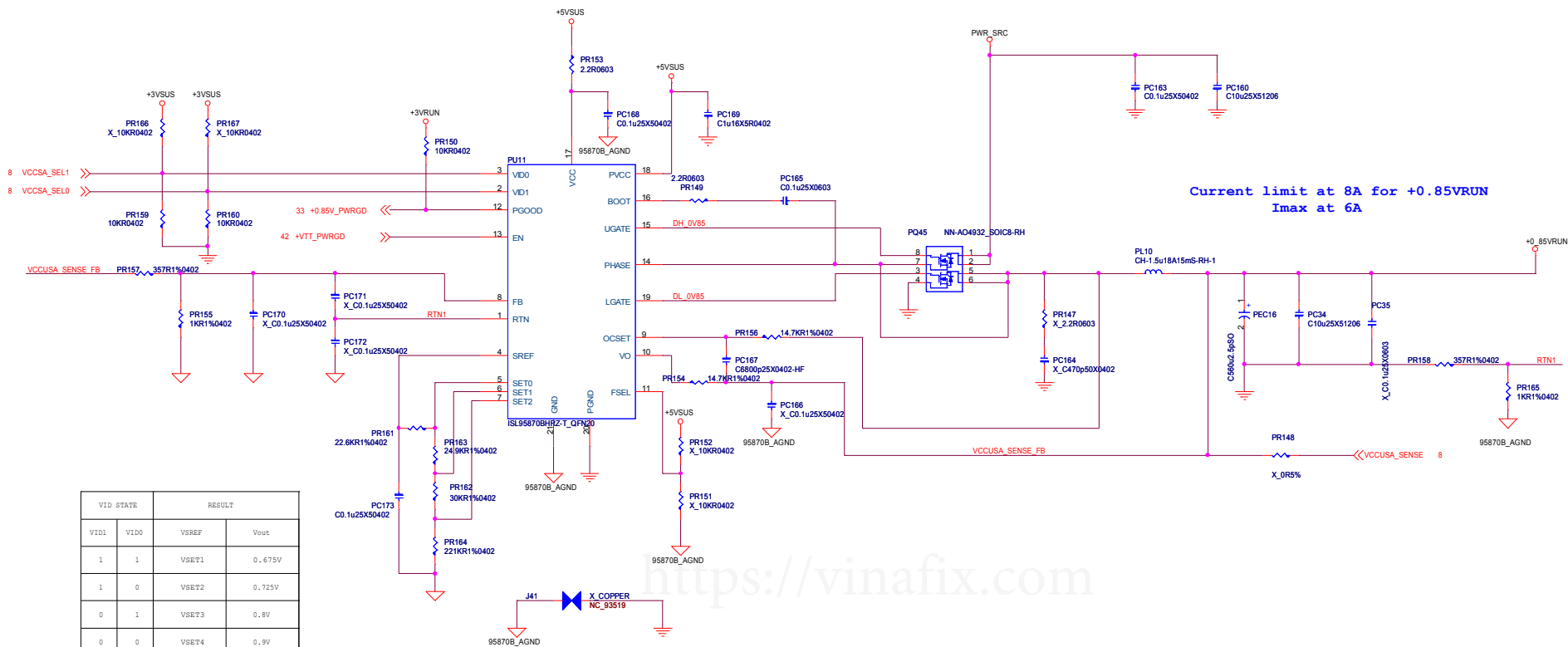


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Title			
<b>DIMM 1.5VRUN</b>			
Size	Document Number		Rev
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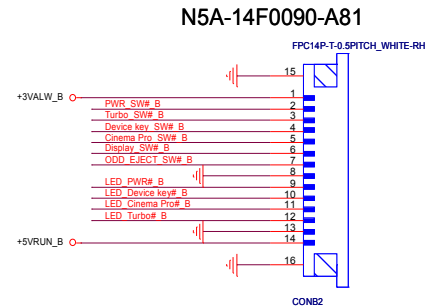
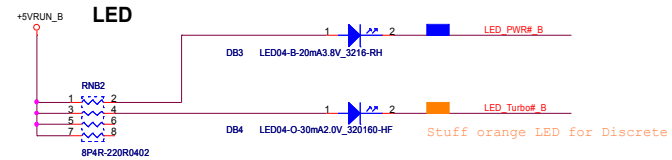
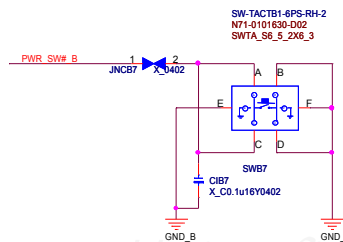
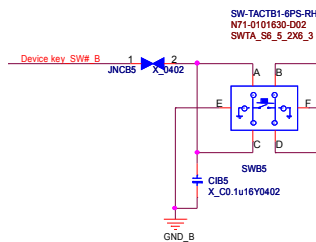
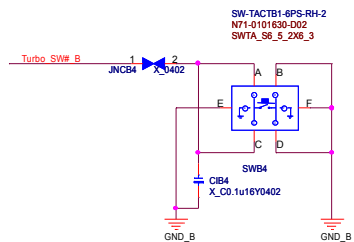
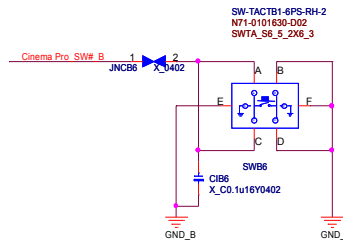
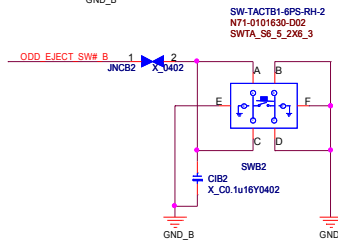
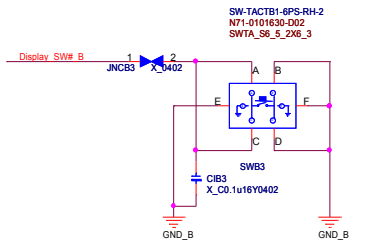
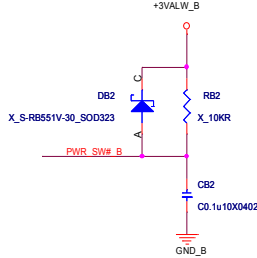




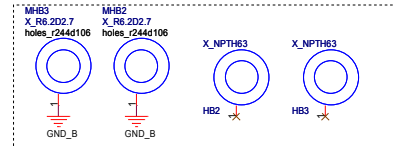








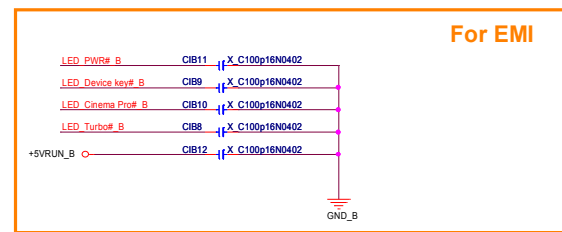
#### SCREW HOLES



E2P-4820111-Y42

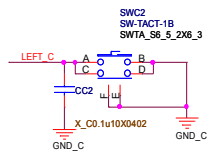


E2Y-4820111-Y42

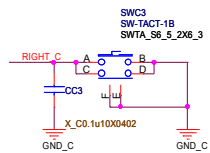


MSI MICRO-STAR INT'L CO.,LTD.	
Title <b>Launch Board</b>	
Size Custom	Document Number <b>MS-14851</b>
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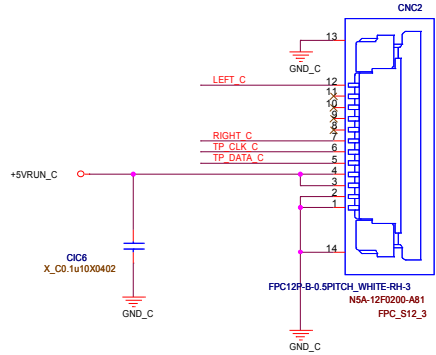




N71-0101630-D02



N71-0101630-D02



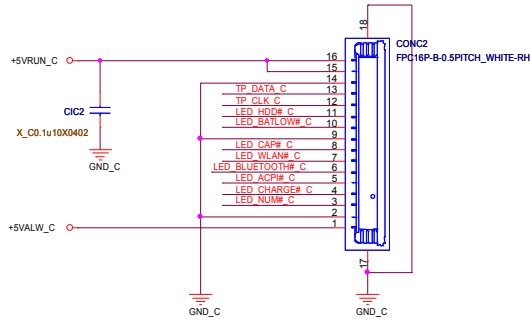
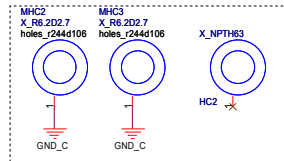
For S8048D-3200 multi finger pin define



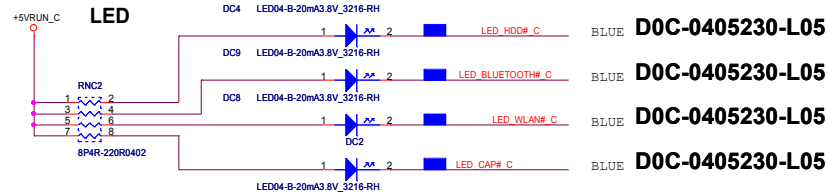
2010/03/29 Add TP board Mylar for ME

E2P-4811811-Y42

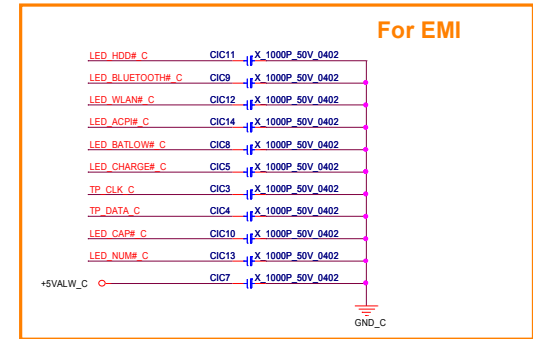
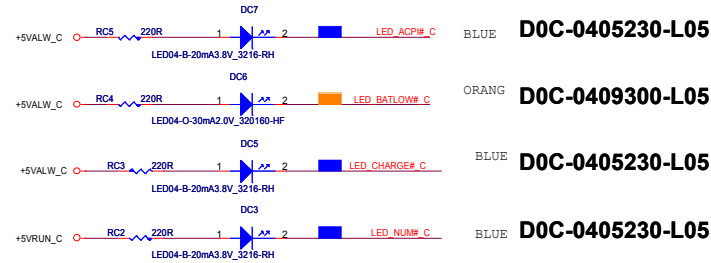
#### SCREW HOLES



N5A-16F0110-A81



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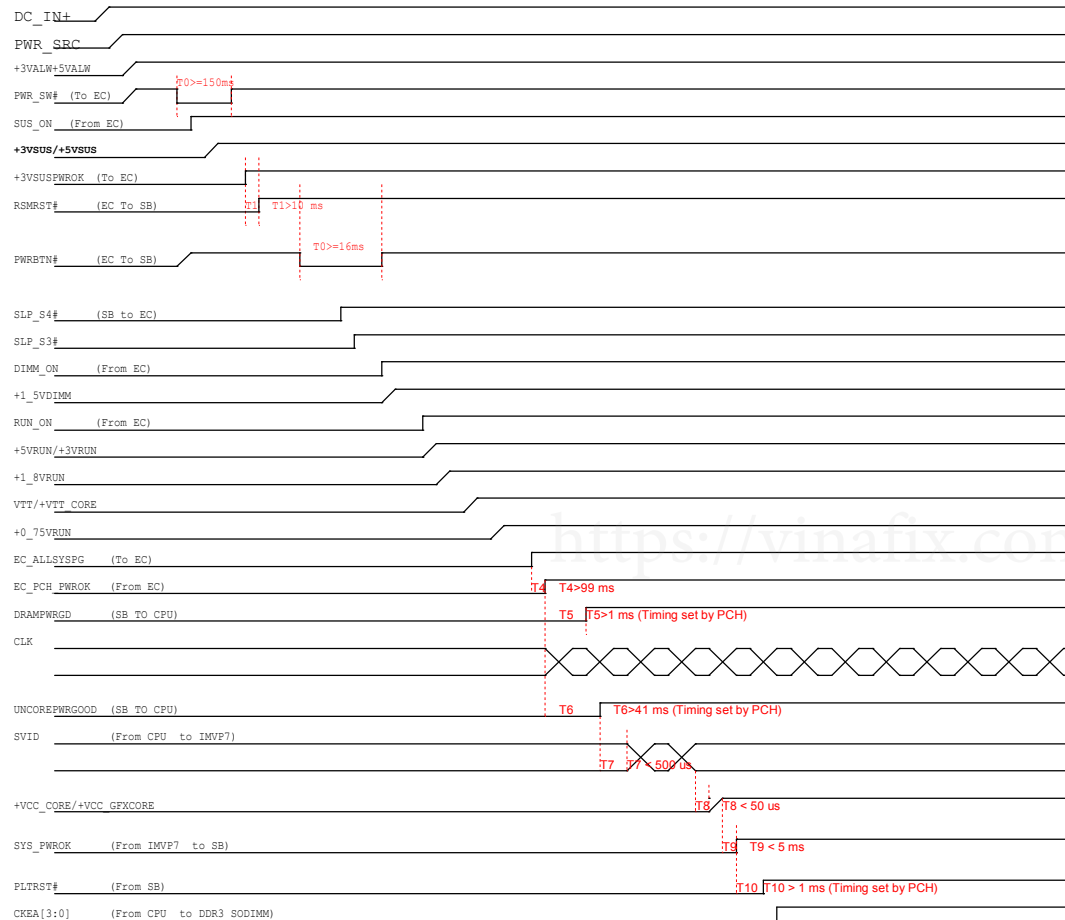


MSI Micro-Star International Co., Ltd.			
MICRO-STAR INT'L CO.,LTD.			
Title: TP,LED Board			
Size: Custom	Document Number: MS-14851		Rev: 10
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# S5-S0

EC programming timing

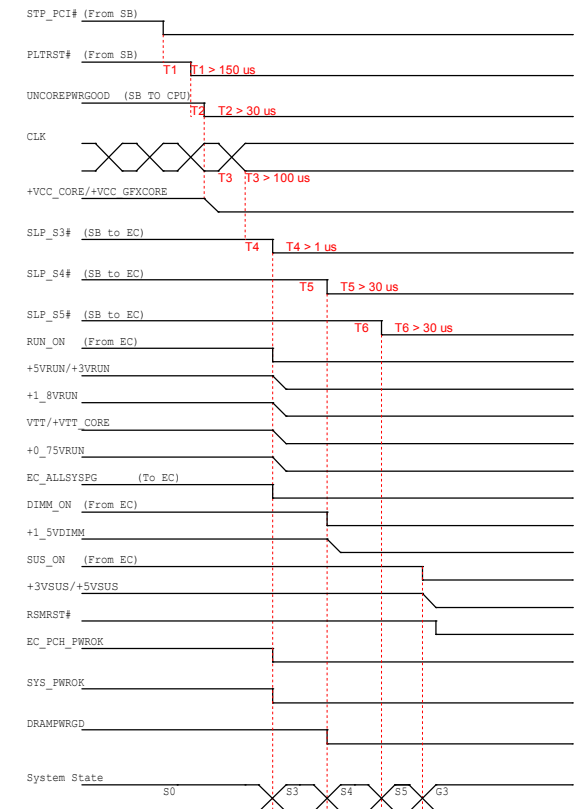
Intel Huron River timing SPEC



# S0-S5

EC programming timing

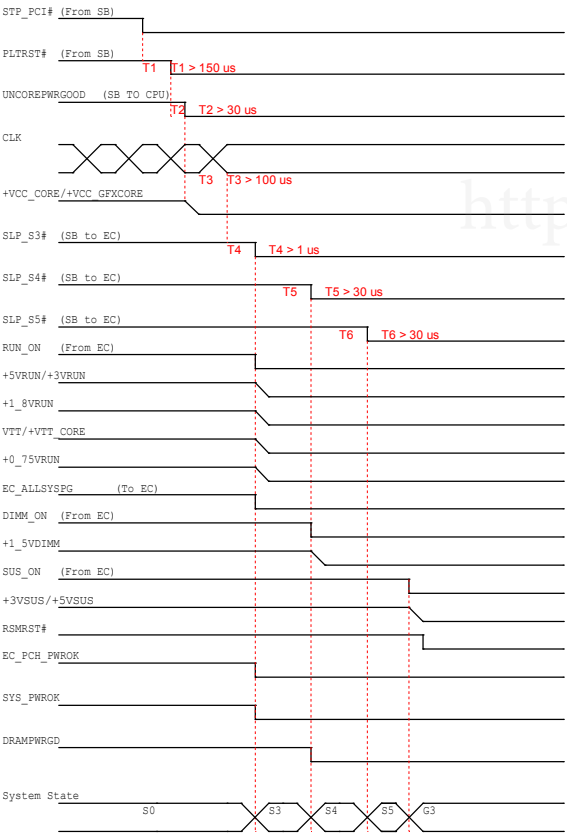
Intel Huron River timing SPEC

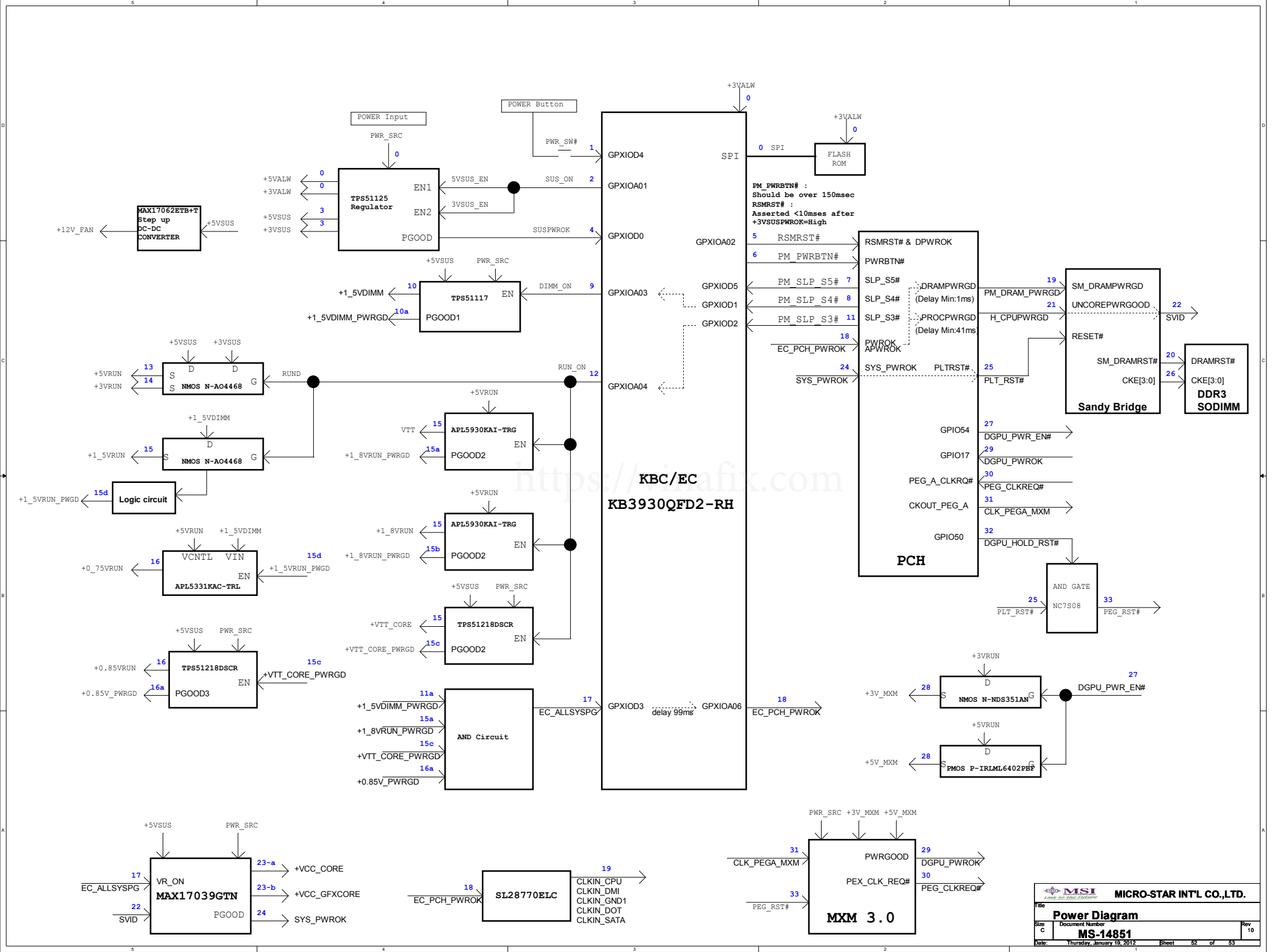


Power down Sequence DC mode S0 to G3

S0-S5

EC programming timing  
Intel Huron River timing SPEC





0B Modify list

- 1, Change power net +1\_5VRUN to +1\_5VDIMM.
- 2, Co-lay PX4.0 and PX5.0.
- 3, Change HDMI CNT footprint to HDMI\_D19\_11.

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Title		
History		
Size A	Document Number <b>MS-14851</b>	Rev 10
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